

```
Model:SKYLAKE-U AIO
PCB Version:-1
PCB Number:14091
PCB P/N:
SCH Version:
ECO# number : 826756
```

PAGE	TITLE	
01	Cover Page	
02	Block Diagram	
03	Reserved	
04	CPU(JTAG/CPU SIDE BAND)	
05	CPU(DDR3L)	
06	CPU_(CFG)	
07	CPU(POWER)	
08	CPU(DISPLAY)	
09	Reserved	
10	CPU(POWER CAP1)	
11	CPU(POWER CAP2)	
12	DDR3_SODIMM1	
13	DDR3_SODIMM2	
14	Reserved	
15	CPU(CSI2/EMMC)	
16	CPU_(PCIe/SATA/USB)	
17	CPU(ACPI/CLK)	
18	CPU(SPI/SMBUS/LPC)	
19	CPU(HDA)	
20	CPU(GPIO/UART/SPI/I2C)	
21	CPU(POWER)	
22	CPU(RSVD)	
23	CPU(VSS)	
24	SIO_IT8739	
25	Flash ROM/RTC	
26	FAN_CIRCUITS/HOLE/THER	
27	AUDIO_ALC3661	
28	AMP_TPA3131	
29	MIC/SPEAKER/AUDIO JACK	
30	Reserved	
31	LAN_RTL8111H	
32	RJ45+Transformer	
33	CardReader_CONN	
34	USB2.0_CONN	
35	USB3.0_CONN	
36	EC_NPCE948L	
37	USB_Charger_(RES)	
38	WEBCAM	
39	Reserved	
40	RUN_PWR/USB_PWR	
41	DSW_POWER_CTL	
42	DC_IN/BATT_CONN	
43	Reserved	
44	CHARGER(BQ24727)	
45	RT8243BZQW_5V/3D3V	
46	NCP81206MN_CPU_VCORE(1/3)	
47	NCP81206MN_CPU_VCORE(2/3)	
48	NCP81206MN_CPU_VCCGT(3/3)	
49	(Reserved)	
50	NCP81253MN_CPU_VCCSA	
51	MEM&MEMVTT_RT8207P_1D35V	
52	DCDC-1DV/VCCIO/VCCPRIM	
53	LDO_APL5930KAI_1D8V	
54	Reserved	
55	SCALAR	
56	HDMI_IN	
57	HDMI_OUT	
58	Panel Control	

[illegible]

```
BOM Configuration
(R_):UNMOUNT
(G_):GPU
(U_):UMA
(T_):TOUCH
(C_):REAR IO CONN(non-battery)
(X_):XDP & DEBUG USE(REMOVE AT 1A)
(D_):DEBUG USE(REMOVE AT MP)
(B ):BATTERY
```

PCB BOARD SIZE

185mm X 230mm

SA BUILD

Intel SKL-U Platform

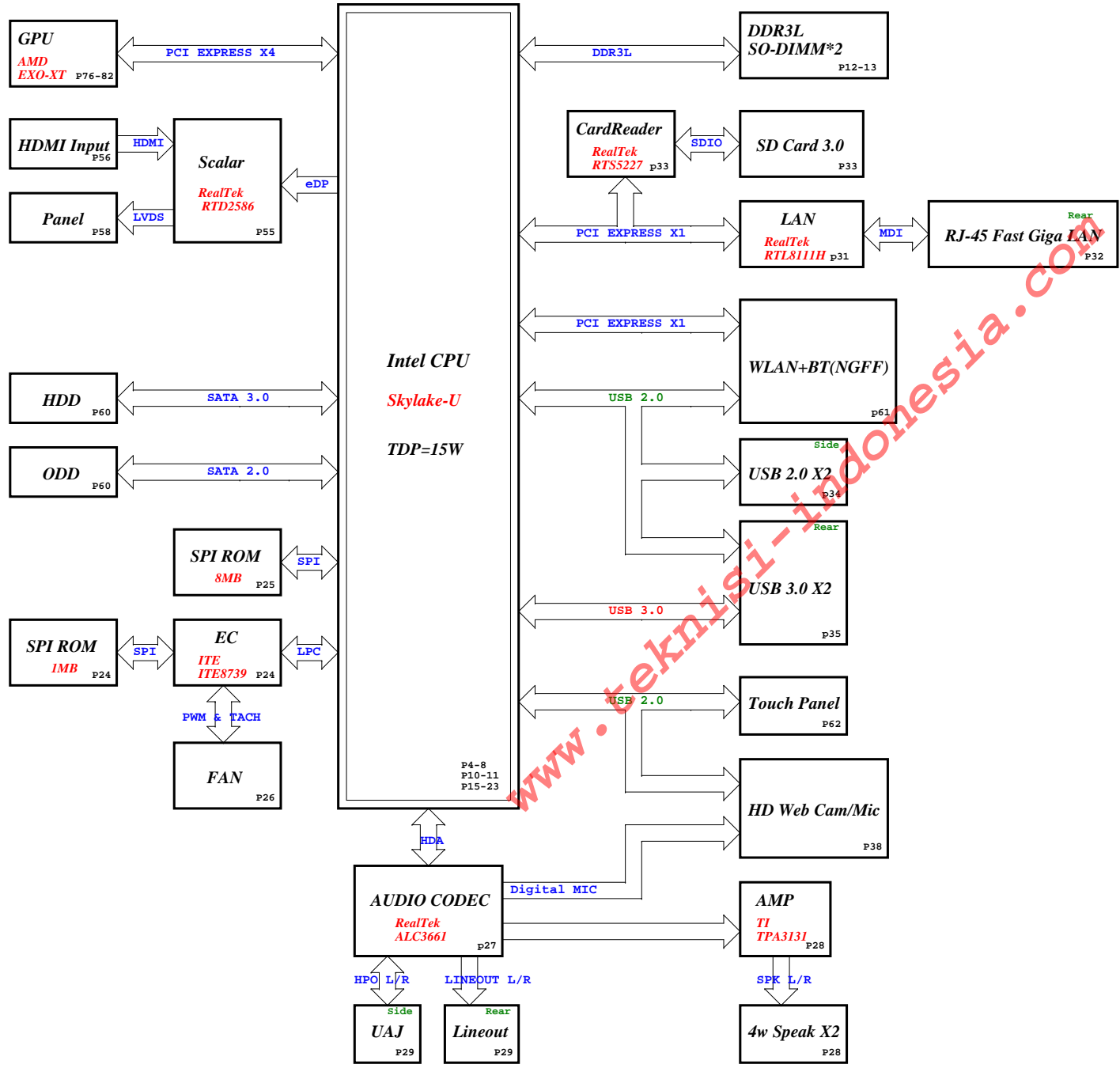
LAN : Gb LAN RTL8111H

AUDIO: ALC3661

SIO EC:ITE8739

Project Name: Jasmine-SKL-U AIO
Project Code: 3PD026010001
PCB Version: -1
PCB Number :14091

PCB BOARD SIZE
185mm X 230mm
6 Layer



CHARGER		P44
BO24727RGR	INPUTS	OUTPUTS
DC_19V	DCBATOUT	BT+
SYSTEM DC/DC		P45
RT8243BZQW	INPUTS	OUTPUTS
DCBATOUT	V_5P0_A	V_3P3_A
CPU Core Power		P46-50
NCP81206MNTXG	INPUTS	OUTPUTS
DCBATOUT	VCC_CORE	1V_VCCGT
	1V_VCCGT	1V_VCCGA
DDR3L Power		P51
RT8207PGQW	INPUTS	OUTPUTS
DCBATOUT	1D35V_S3	V_OP675_S3
CPU1V and switch		P52
RT8237CZQW	INPUTS	OUTPUTS
DCBATOUT	1D0V_S5	1V_VCCIO
SYSTEM 1D8V		P53
APL5930KA1	INPUTS	OUTPUTS
SB3V	1D8V_S5	
PANEL BL POWER		P59
OZ554ALN	INPUTS	OUTPUTS
DCBATOUT	VOUT_INV	
GPU CORE POWER		P83
ISL62882CHRTZ-T	INPUTS	OUTPUTS
DCBATOUT	VGA_CORE	
GPU 0D95V/1D8V POWER		P84
RT8068AZQW	INPUTS	OUTPUTS
RT8068AZQW	SB3V	0D95V_VGA_S0
	DCBATOUT	PWR_1D8V
SWITCH		P41-42
	INPUTS	OUTPUTS
	V_5P0_A	VCC
	V_3P3_A	VCC3
	V_5P0_A	SB3V
	V_3P3_A	SB3V
PCB LAYER		
L1:TOP		
L2:GND		
L3:SIGNAL/POWER		
L4:SIGNAL/POWER		
L5:GND/POWER		
L6:BOTTOM		

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

File

002_Block Diagram

Size

C

Document Number

Rosa_SKL-U AIO

Date

Monday, August 17, 2015

Sheet

2 of 105

Rev

-1

Blanking

www.teknisi-indonesia.com

<Variant Name>



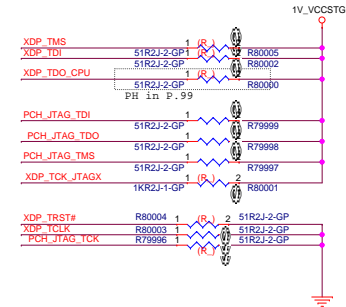
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title 003_(Reserved)

Size A	Document Number Rosa_SKL-U AIO	Rev -1
-----------	-----------------------------------	-----------

Date: Wednesday, July 01, 2015 Sheet 3 of 105

```
#543016 Rev0.7: Ra = 500 ohm / Rb = 1k ohm
#544669 Rev0.52:
Ra = 56 ohm (TO BE CHANGED TO 100 OHMS) / Rb = 62 ohm and 150 ohm
```

[illegible]

L NORMAL (DEFAULT)
 H Disable

CNTL2
 (84.T3906.E11)
 RBT3906-4-GP
 544
 R153
 1KR2J-1-GP
 2 1
 AUD_LINK_SDO_R1
 SB3V 0
 ME1
 JOWLE-CON2-5-GP
 (21.82874.102)

Pin Name	Schematic Notes
DDR0_ODT[1:0]/ DDR1_ODT[1:0]	No Connect at processor side
ODT[1:0]	SO-DIMM connector ODT[1:0] pins tied to VDDQ through a FET and a resistor.

Main Func = CPU

12 M_A_DQ[63:0] <<<
12 M_A_A[15:0] <<<
12 M_A_DQS_DN[7:0] <<<
12 M_A_DQS_DP[7:0] <<<

DDR3L ball type: Non-Interleaved Type

13 M_B_DQ[63:0] <<<
13 M_B_A[15:0] <<<
13 M_B_DQS_DN[7:0] <<<
13 M_B_DQS_DP[7:0] <<<



<Variant Name>

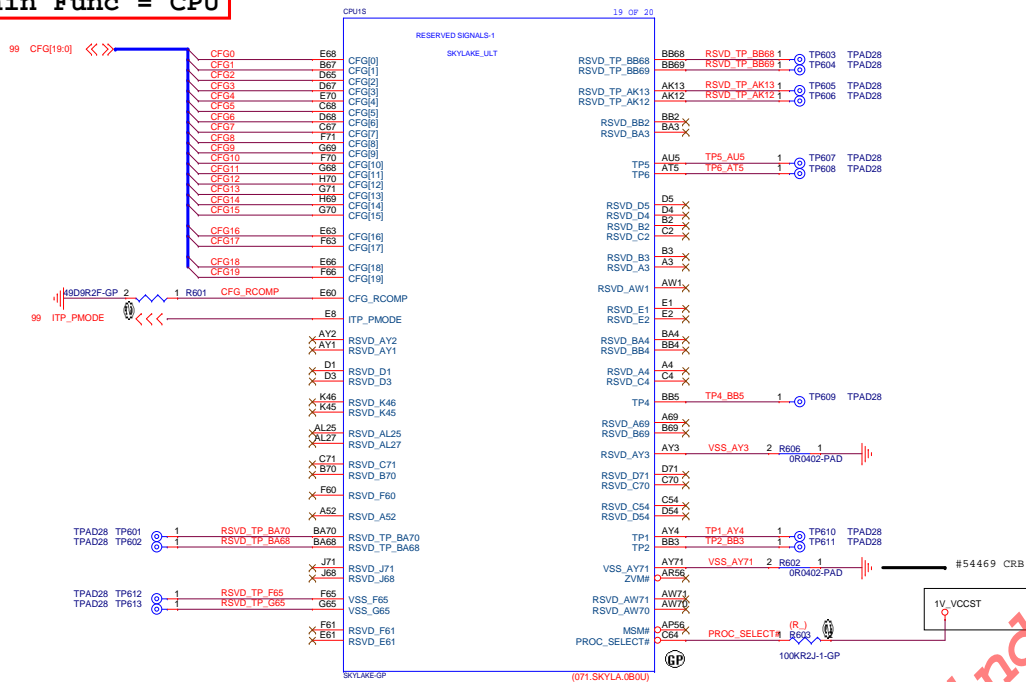
w!stron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

File 005_CPU(DDR3L)(NEW)

Size C	Document Number Rosa_SKL-U-AR	Rev -1
Date:	Wednesday, July 01, 2015	Sheet 5 of 105

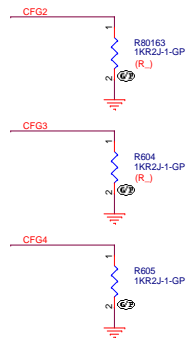
Main Func = CPU



Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB71	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	Corner A1
C1	NCTFVSS	Test Point (TP)	
A5	NCTFVSS	Test Point (TP)	Corner A71
A70	NCTFVSS	Test Point (TP)	
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

PCH strap pin:



[BDW Only] PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX_ENABLED BIT IN DEBUG_INTERFACE MSR
	1 : DISABLED

(#543016)

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port.
	1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

SKL (#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

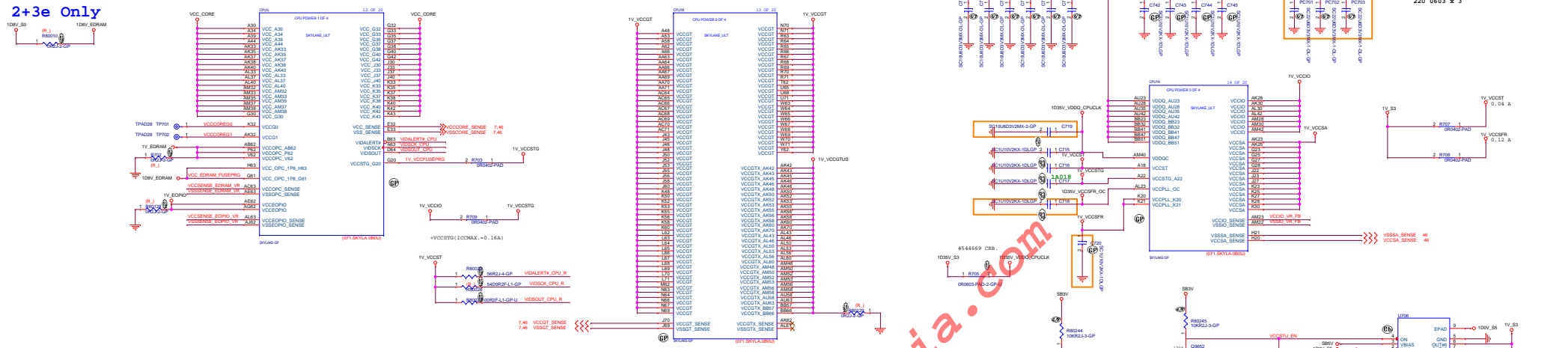
<Variant Name>

wlstron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title 006_CPU_(CFG)			
Size C	Document Number Rosa_SKL-U_AK		Rev -1
Date:	Wednesday, July 01, 2015	Sheet	6 of 105

Main Func = CPU

+V_EOPIO_VR and +V_EDRAM_VR powere source from 1D0V_S0

2+3e Only



SVID_543016:

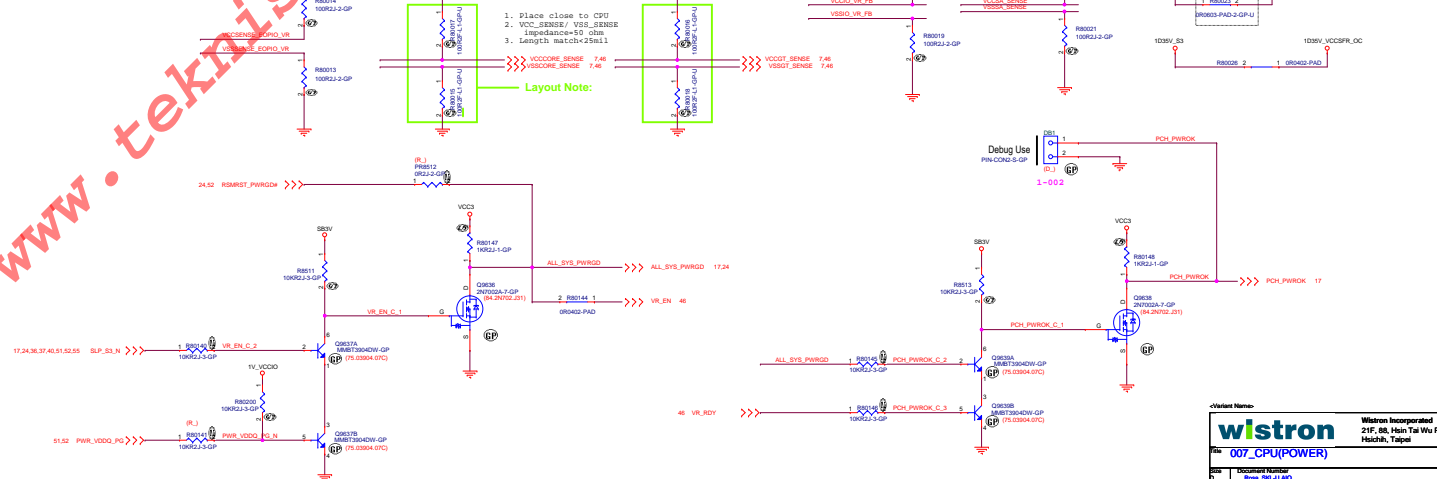
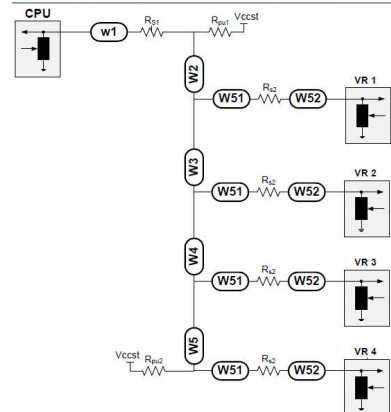


MANAGEMENT RAIL POWER GENERATION

Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2 + W3 + W4 + W5 [inches]	W51 [inches]	W52 [inches]	R _{REQ} [Ω]	R _{REQ} [Ω]	R _{S1} [Ω]	R _{S2} [Ω]	V _{CC} PT [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

Figure 10-7. Routing Illustration for SVID Topology



Main Func = CPU

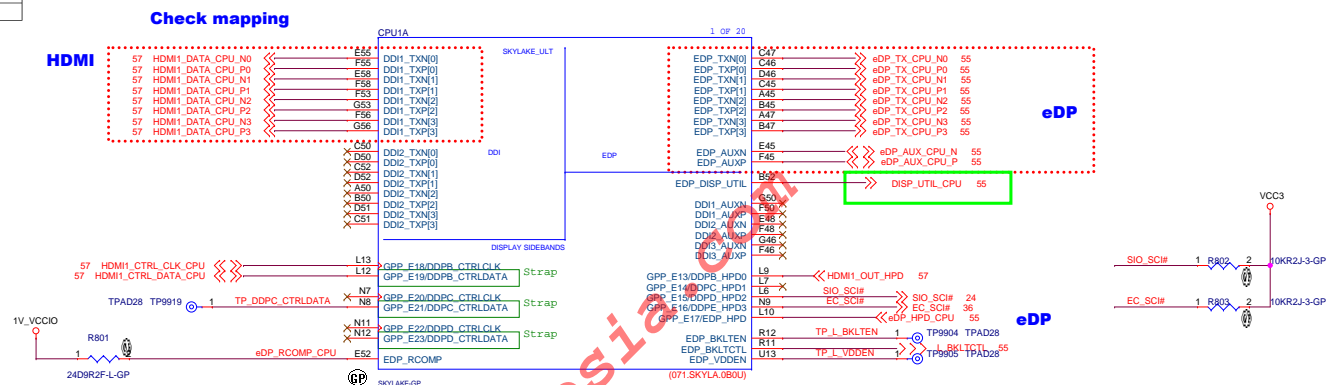
Table 5-10. DDI Disabling and Termination Connections

Pin Name	Recommendation
DDPB_AUXP DDPB_AUXP	No Connect
DDPB_AUXN DDPB_AUXN	No Connect
DDPB_HPD DDPB_HPD	No Connect
DDI1_TXP[3:0] DDI2_TXP[3:0]	No Connect
DDI1_TXN[3:0] DDI2_TXN[3:0]	No Connect
DDPB_CTRLCLK DDPB_CTRLDATA	No Connect
DDPC_CTRLCLK DDPB_CTRLDATA	No Connect

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

These two signals have weak internal pull-down.



Blanking

www.teknisi-indonesia.com

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title **009_(Reserved)**

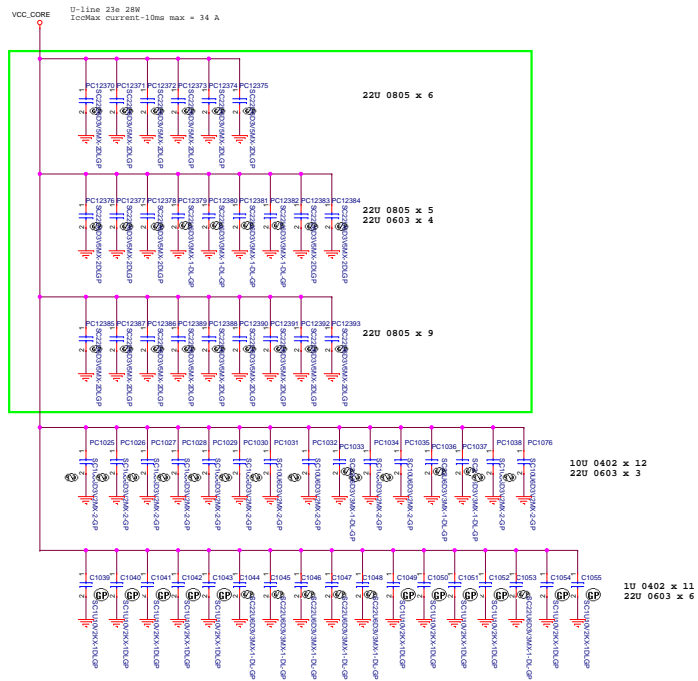
Size Document Number
B Rosa_SKL-U AIO

Rev
-1

Date: Wednesday, July 01, 2015 Sheet 9 of 105

Main Func = CPU

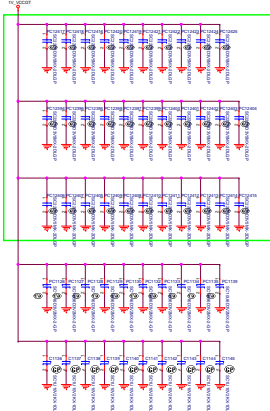
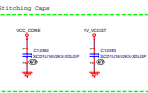
CORE CAP follow Cap_Sorting list



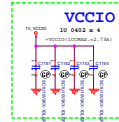
www.teknisi-indonesia.com

- Support for power sequencing signals as described in the Skylake Platform Intel® Management Engine (Intel® ME) and Embedded Controller (EC) Interaction - Product Specification.

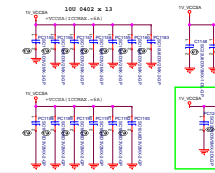
```
U-line 230 20W
IocMAX current=1000 max[A] = 67 A
```

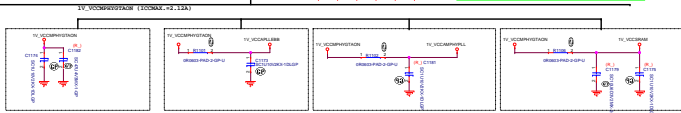

$$I_{V_VDDPTE}(V_{DDPTE}) = (I_{DCHNL} + I_{LKA})$$


Put on Top	Put on Bottom

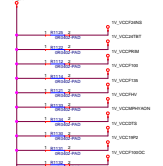


TV_M003A 100 0402 x 13 TV_M003A

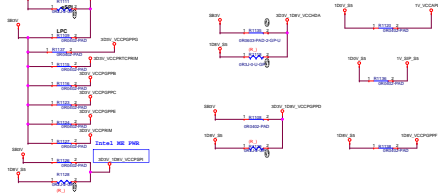




1204/98



10kV_5A 30kV_10kV_VCCPGPPA =VCCPGPPA(2CONAZ,=0,0.6A)

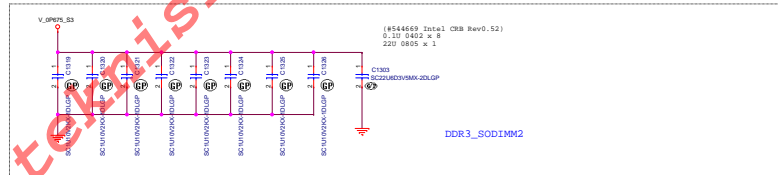
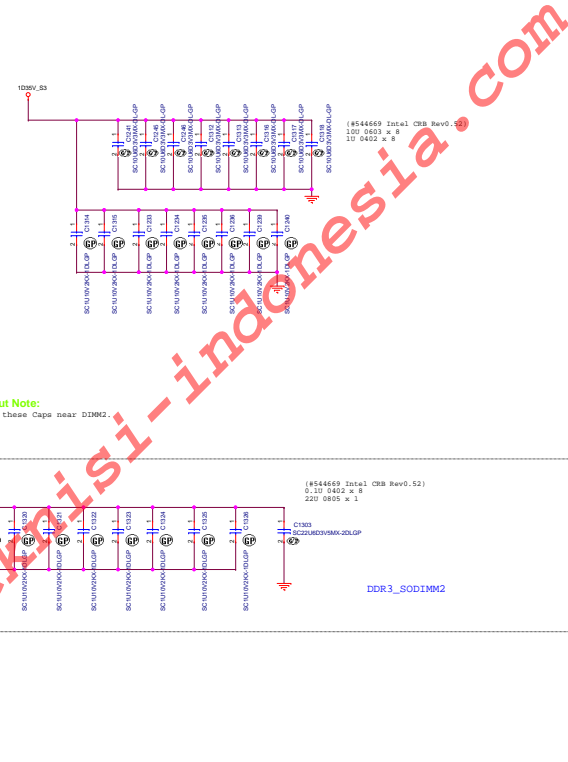
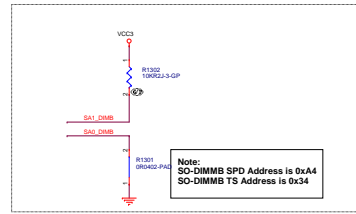
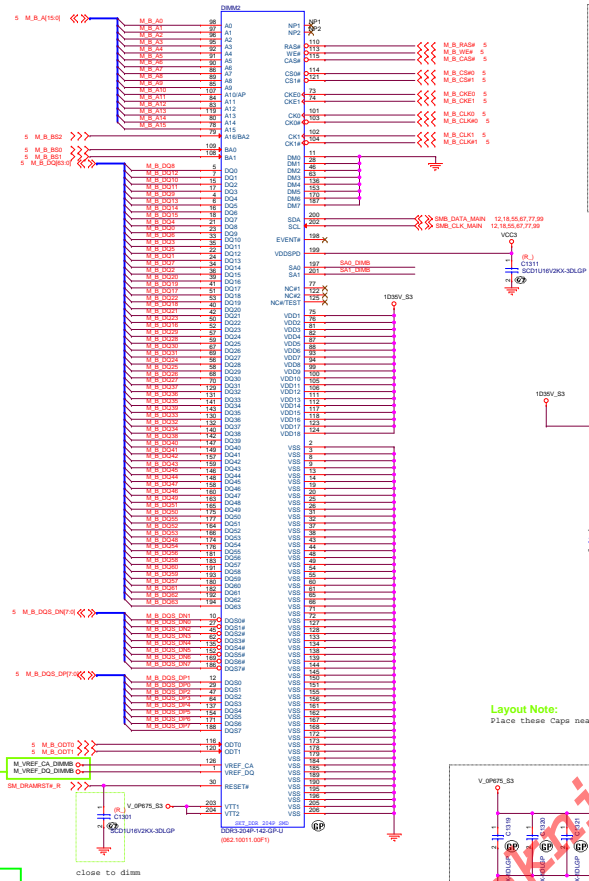
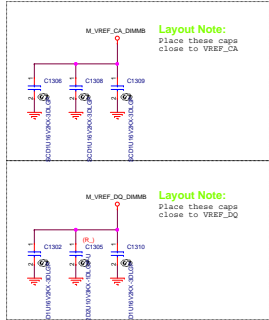


www.teknisi-indonesia.com

www.teknisi-indonesia.com



Main Func = DDR SODIMM



Blanking

www.teknisi-indonesia.com

<Variant Name>



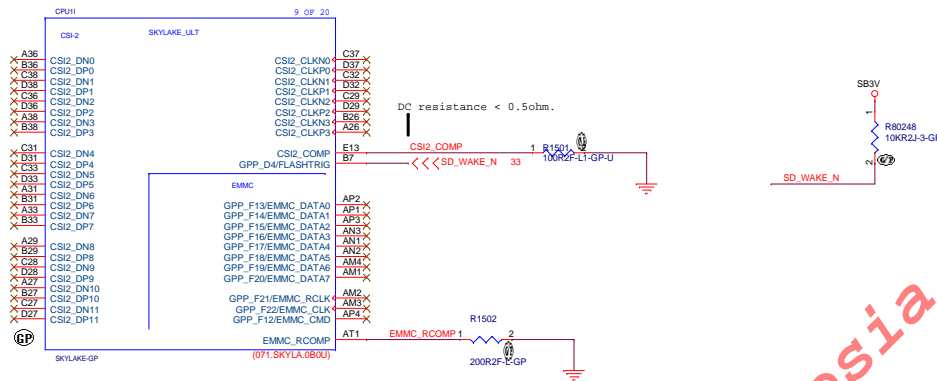
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title **014_(Reserved)**

Size A4	Document Number Rosa_SKL-U AIO	Rev -1
------------	--	-----------

Date: Wednesday, July 01, 2015	Sheet 14 of 105
--------------------------------	-----------------

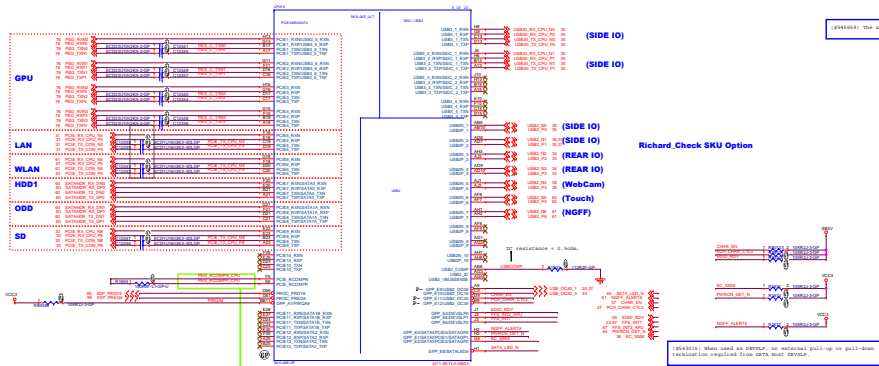
Main Func = PCH

[illegible]

Main Func = PCH

*SATA Port 1 can be configured to PCIe Port 8 or 11
Not all ports are available on all SKUs

Richard Check PCIe Config



18454001: The HSI0 controller supports 100 Mbps port on all HSI0.0 capable ports

Richard Check SKU Option

TBD

Table 24-3. PCI Express® Link Configurations Supported

SKL	PCIe Link Config	PCI Express® Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3		Port5		Port7		Port9		Port11	
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3		Port5		Port7		Port8			
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2	Port1		Port3		Port5		Port7		Port9			
	2x1	Port1		Port3		Port5		Port7		Port9	Port10		

PCIe Port1	PCIe Port2	PCIe Port3	PCIe Port4	PCIe Port5	PCIe Port6	PCIe Port7	PCIe Port8	PCIe Port9	PCIe Port10	PCIe Port11	PCIe Port12
1	2	3	4	5	6	7	8	9	10	11	12

PCIe Table

Port	Device	Share Bus
1	X	
2	X	
3	X	
4	X	
5	WLAN	PCIe
6	LAN	PCIe
7	WIO	SATA
8	ODD	SATA
9	SSD	PCIe
10	SSD	PCIe
11	SSD	PCIe
12	SSD	PCIe/SATA

USB 2.0 Table

Port	Device
1	USB2.0 Port1
2	USB2.0 Port2 (Debug Port)
3	USB2.0 Port3 (IO Hub)
4	USB2.0 Port4 ODMA_5
5	X
6	WLAN
7	Touch Panel
8	Card Reader
9	X
10	X

USB 3.0 Table

Port	Device
1	USB3.0 Port1 ODMA_3
2	USB3.0 Port2 ODMA_3 (Debug Port)
3	20 GMSB
4	X
5	X
6	X

Notes:

1. 1000 Mbps - 4 wire (breakout) 10-15 mHz (trans)
2. 1000 Mbps - 4 wire (breakout) 10-15 mHz (trans)
3. 1000 Mbps - 4 wire (breakout) 10-15 mHz (trans)
4. 1000 Mbps - 4 wire (breakout) 10-15 mHz (trans)
5. 1000 Mbps - 4 wire (breakout) 10-15 mHz (trans)
6. 1000 Mbps - 4 wire (breakout) 10-15 mHz (trans)
7. 1000 Mbps - 4 wire (breakout) 10-15 mHz (trans)
8. 1000 Mbps - 4 wire (breakout) 10-15 mHz (trans)
9. 1000 Mbps - 4 wire (breakout) 10-15 mHz (trans)
10. 1000 Mbps - 4 wire (breakout) 10-15 mHz (trans)
11. 1000 Mbps - 4 wire (breakout) 10-15 mHz (trans)
12. 1000 Mbps - 4 wire (breakout) 10-15 mHz (trans)

18454001 (SCL_PCH_V_004 Rev0.1)

18454001: When used as 100Mbps, no external pull-up or pull-down is required. When used as 100Mbps, no external pull-up or pull-down is required.

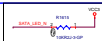


Figure 3-1. HSI0 Muxing on SKL PCH-LP (U Series)

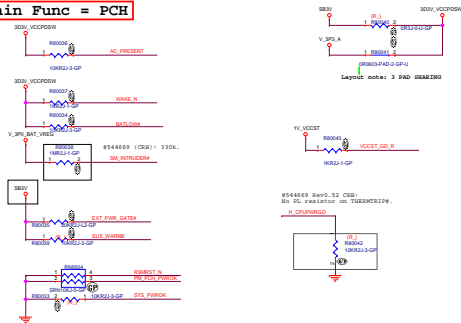


Overcurrent Pin Default Usage_543016

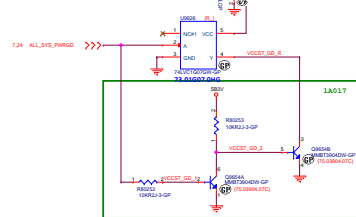
Notes: GBE is for Intel LAN chip only.

www.teknisi-indonesia.com

Main Func = PCH

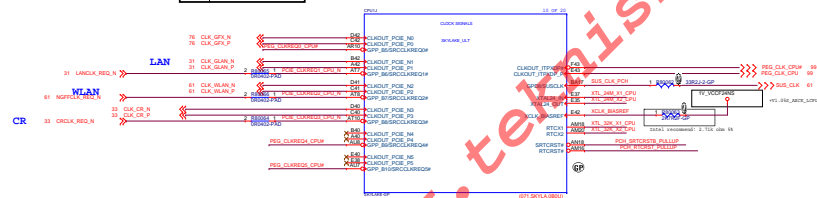


VCCST_PWRGD / HWM201:

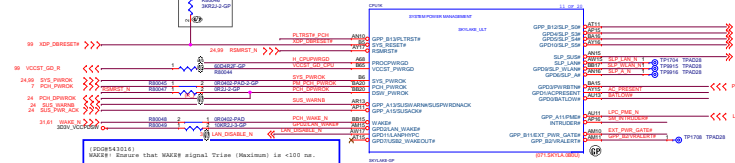
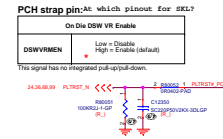


CLK OUT Table

Pair	Device
0	Reserved
1	SSD(RQ1#)
2	LAN(RQ2#)
3	WLAN(RQ3#)
4	Reserved
5	Reserved



GPP_A13-15 pin(LPC/eSPI)



PASSWORD CLEAR

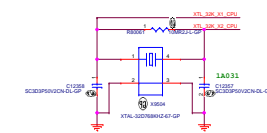


APS_Pin3&7:

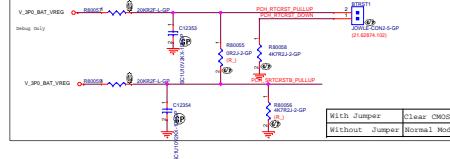
#543616 Rev0.7

1. VCCST_FWRGD is only 1.8 V tolerant.
2. VCCST_FWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST.

APS_543016



CLEAN CMOS



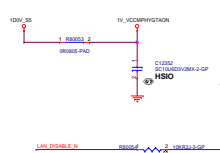
VCCST_PWRGOOD



- **VCCST_PWRGOOD** is a signal on the processor that indicates both the **VCCST power supply** and **VDDQ power supply** are within voltage tolerance specification

4	MSL_SLP_00_N	WHEN ASSERTED (0): SYSTEM IS IN S0	7.004	0
5	MSL_SLP_04_N	WHEN ASSERTED (0): SYSTEM IS IN S4	7.008	11
6	MSL_SLP_06_N	WHEN ASSERTED (0): INTO PE TO HOFF	7.004	24
7	MSL_SLP_07_N	USED TO DETERMINE IF SYSTEM IS IN DEEP S4/S0	7.004	25
14	GRD	Ground for SYS_RESET		
15	SLP_0#	When asserted (1) system is in deterministic idle state		
16	NC	No Connection		
17	NC	No Connection		
18	NC	No Connection		

+VCCMPHYGTAON_1P0(ICCMAX.=3.5A)



PCH strap pin:

DCH Prim

PCH strap pin:

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

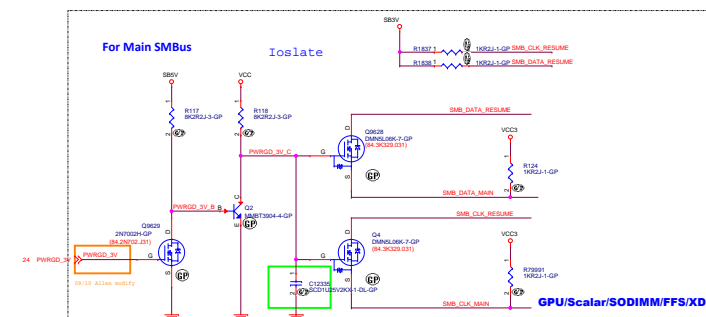
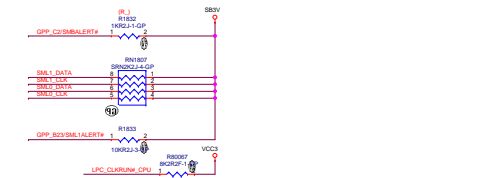
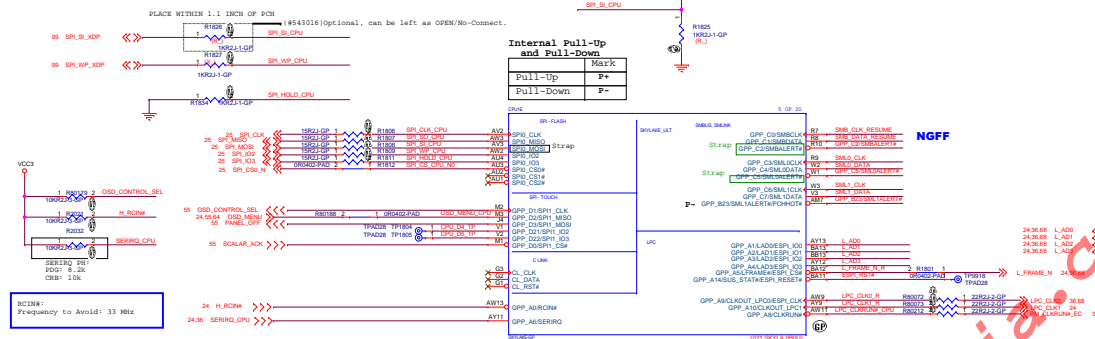
This signal has a weak internal pull-up.

PCH strap pin:

TLS Confidentiality

SMBALERT# / GPP_C2	<ul style="list-style-type: none"> Low = Disable Intel ME Crypto TLS (Default) High = Enable Intel ME Crypto TLS
--------------------	--

The internal pull-down is disabled after RSMRST# deasserts.



Main Func = PCH

Card Reader by SDIO_545659:

PCH strap pin:

Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs

DMIC Table

Pair	Device
0	DMIC Port1
1	DMIC Port2

PCH strap pin:

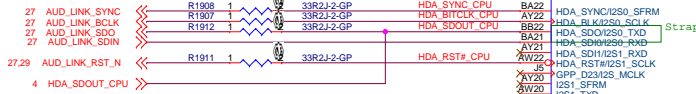
Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default High = Enable

The internal pull-down is disabled after PLTRST# deasserts

SD3V_1D8V_VCHDA



AUDIO

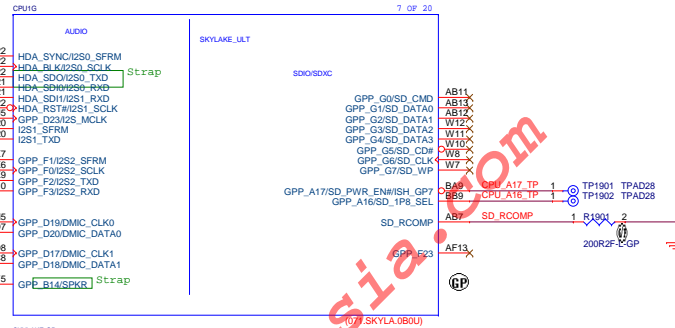
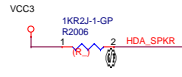


DMIC

PCH strap pin:

Top Swap Override	
HDA_SPKR	Low = Disable (Default) High = Enable

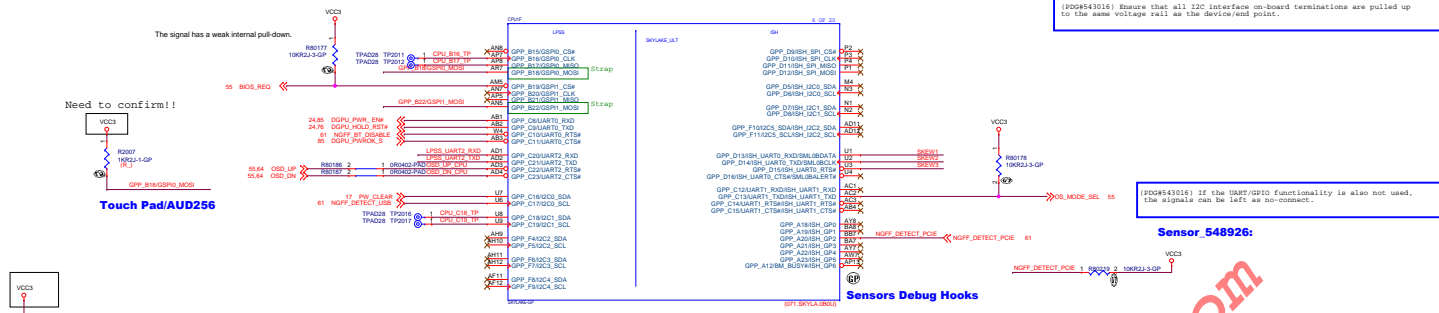
The internal pull-down is disabled after PLTRST# deasserts



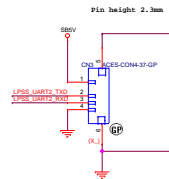
<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title		019_CPU(HDA)	
Size	Document Number	Rev	
C	Rosa_SKL-U AK	-1	
Date:	Wednesday, July 01, 2015	Sheet	19 of 105

Main Func = PCH



Intel has removed BNC1 controller from BSLU and proposed to use USB/UART Muxing for Win7 debug.



PCH strap pin:

Boot BIOS Strap Bit BBS
Boot BIOS Destination
Low = GPU (Default)
High = LPC

The internal pull-down is disabled after PLTRST# deasserts

Need double confirm, GPIO table set to GPI if that's needed PE or PL

Skew ID Settings

MB Version	Skew1	Skew2	Skew3
GPU	0	1	1
UMA	0	0	1
GPU Touch	0	1	0
UMA Touch	0	0	0

eSPI_508740:



Voltage Supply	Area	PCB Pining showing power rail	Value	Size	Quantity	Placement type (X/Yway / 1/Edge)	Place capacitor(s) near ball(s)
V1.0A / V2.4A	VocPRIM	AK20	-	-	-	-	-
V3.3A	VocPRIM	V19, AJ21	1 uF	0402	1	E (<3 mm)	V19 (Note 1)
	VocGRPB	AG15	1 uF	0402	1	E (<3 mm)	AG15 (Note 1)
	VocGRPC	Y16	1 uF	0402	1	E (<10 mm)	Y16 (Note 1)
	VocGRPE	T16	1 uF	0402	1	E (<10 mm)	T16 (Note 1)
V3.3A / V1.5A / V1.8A	VocDA	AJ19	1 uF	0402	1	E (<10 mm)	AJ19 (Note 1)
V3.3A / V1.5A	VocSPI	AJ16	-	-	-	-	-
	VocGPAA	AK15	-	-	-	-	-
	VocGRPD	Y15	-	-	-	-	-
	VocGGPG	AD15	-	-	-	-	-
	VocTRPCRM	AK17	1 uF	0402	1	E (<3 mm)	AK17
V3.3D5W (2-3A) / V3.3B7C (3.3V)	VocDSW	AD17, AD18, AJ17	0.1 uF	0402	1	-	-
	VocRTC	AK19, BB14	1 uF	0402	1	E (<3 mm)	AK19
			0.1 uF	0402	1	-	-
V1.8A	VocGRPF	AF16	-	-	-	-	-
	VocATS	AA1	1 uF	0402	1	E (<10 mm)	AA1
PCB Internal USB	DeoRTC	BB10	0.1 uF	0402	1	E (<3 mm)	BB10
	DcoDSW	AL1	1 uF	0402	1	E (<3 mm)	AL1

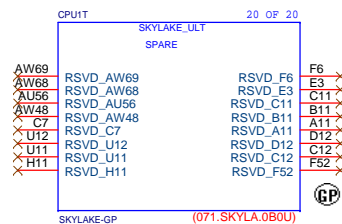
Notes:

- Placeholder only, Does not need to be shielded.
- Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure the shunting is optimized.
- Capacitors should be placed as close as possible to the pins (2-5A) from the edge of package.
- For description of (X/Yway) and (Edge) decoupling capacitor placement, please refer to "Loop Inductance Reduction" section.

Note:

1. Placeholder only. Does not need to be stuffed.
2. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
3. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
4. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to "[Loop Inductance Reduction Decoupling](#)".

Main Func = PCH



www.teknisi-indonesia.com

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

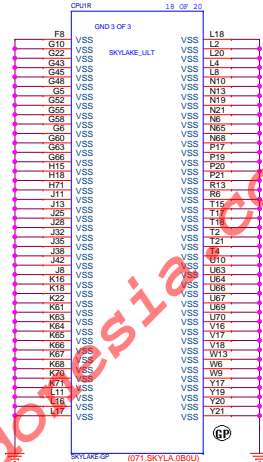
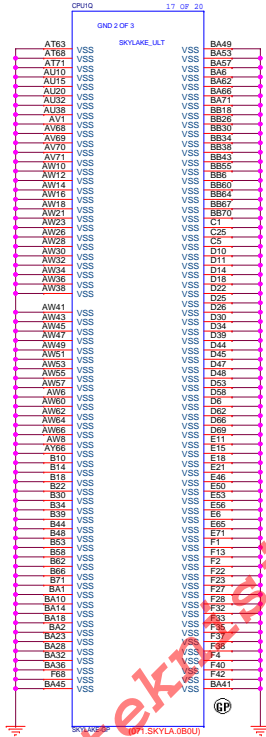
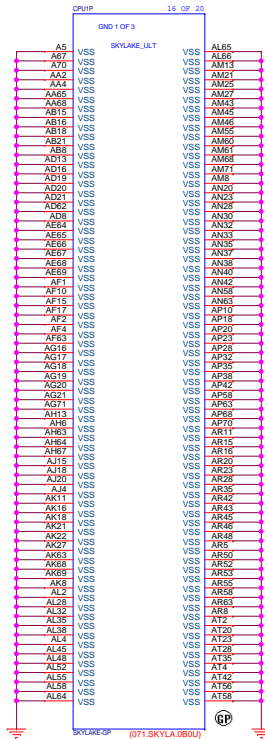
Title 022_CPU(RSVD)

Size A3 Document Number Rosa_SKL-U AIO

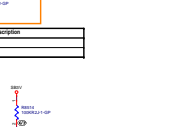
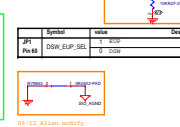
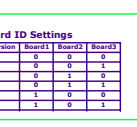
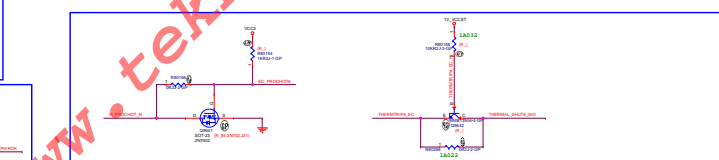
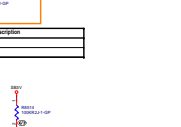
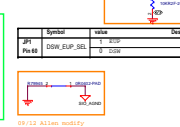
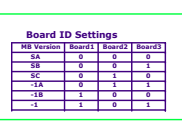
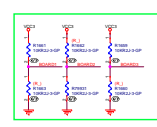
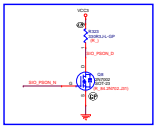
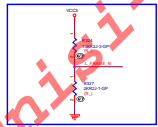
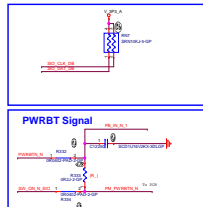
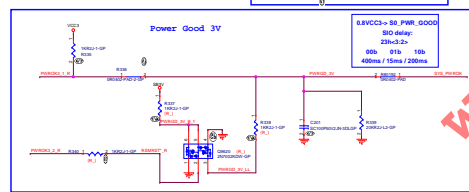
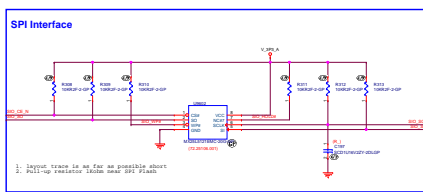
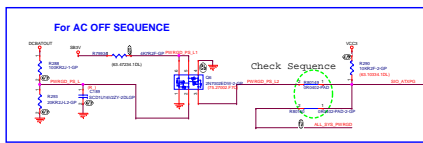
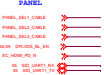
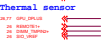
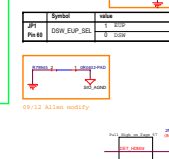
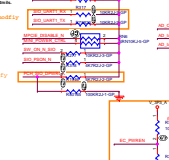
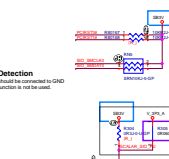
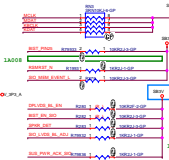
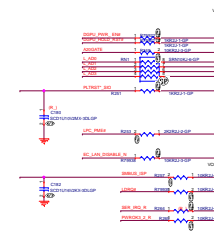
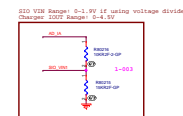
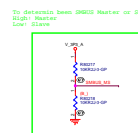
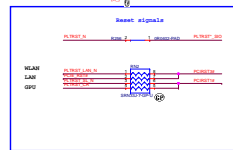
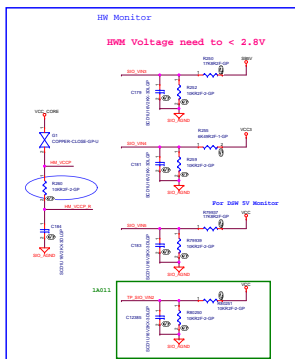
Rev -1

Date: Wednesday, July 01, 2015 Sheet 22 of 105

Main Func = PCH



<Variant Name>



Board ID Settings

Board ID	Board1	Board2	Board3
SA	0	0	0
SB	0	0	1
SC	0	1	0
SD	0	1	1
SE	1	0	0
SF	1	0	1

Case Open Detection

Note: COPEM should be connected to GND when this function is not in use.

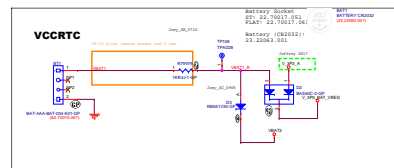
07/22 Alien modify

07/22 Alien modify

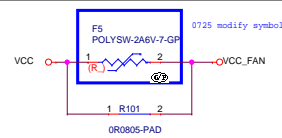
07/22 Power On Strapping Options

Symbol	Value	Description
07	00000000	07/22

07/22 Alien modify



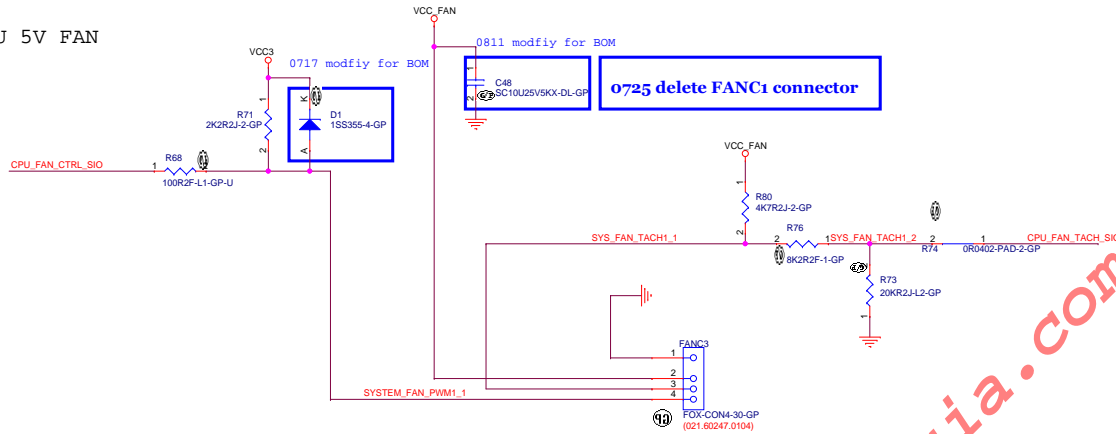
4 PINS FAN CONTROL



CPU 5V FAN

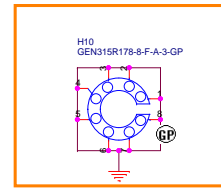
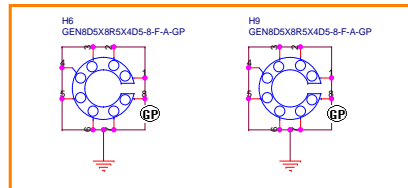
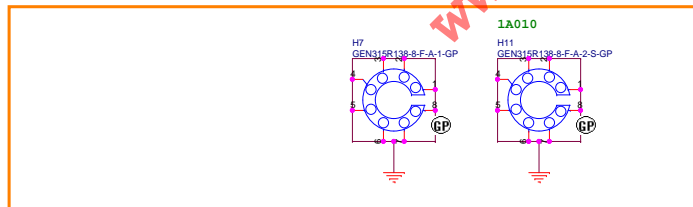
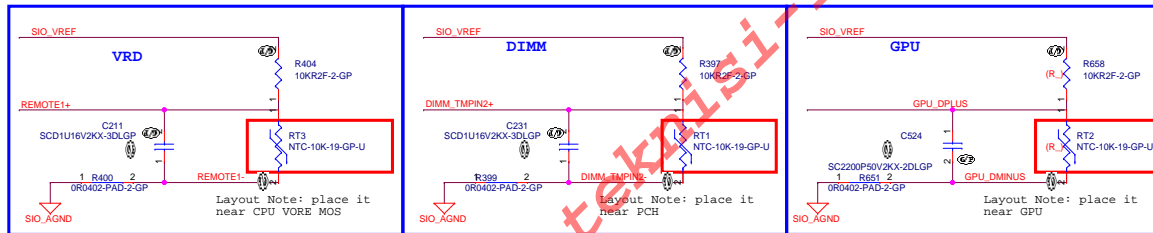
SIO FAN CONTROL

24 CPU_FAN_CTRL_SIO
24 CPU_FAN_TACH_SIO



THERMAL DIODES

24 SIO_VREF
24 REMOTE1+
24 DIMM_TMPIN2+
24.77 GPU_DPLUS
77 GPU_DMINUS

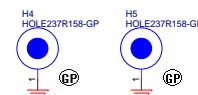


0805 modify screw hole to ZZ.0HOLE.011
0731 add screw hole
0730 delete screw hole
0724 add F7 for BOM
0714 change part

CPU Heatsink screw hole.



GPU Heatsink screw hole.



<Variant Name>

wistron

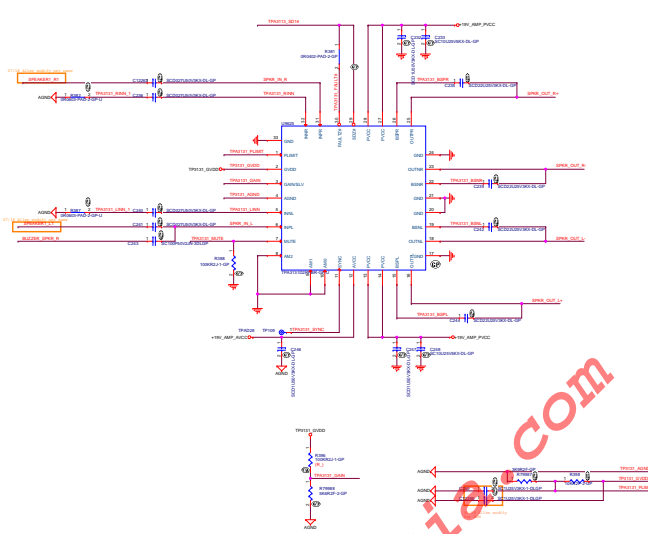
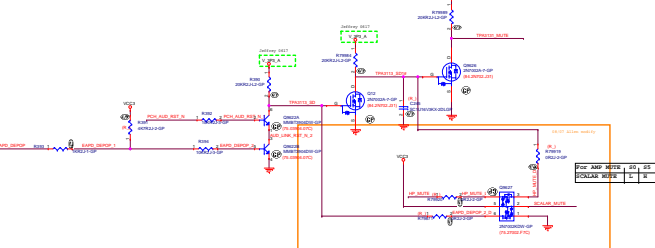
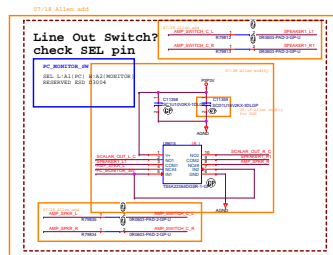
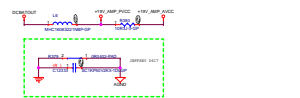
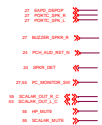
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

File 026_FAN CIRCUITS/HOLE/THER

Size C Document Number
Rosa_SKL-U AIO

Rev
-1

Date: Wednesday, July 01, 2015 Sheet 26 of 105



Internal Speaker x 2

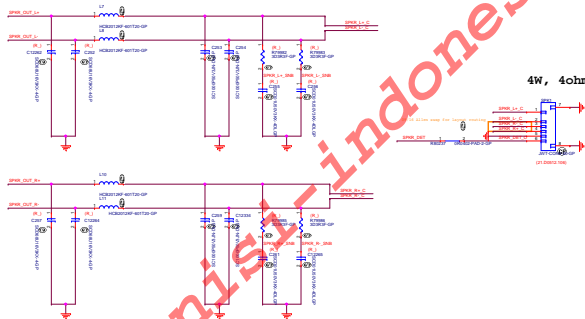


Table 1. GAIN and MASTER/SLAVE

MASTER / SLAVE MODE	GAIN	R1 (to GND) ⁽¹⁾	R2 (to GND) ⁽¹⁾	INPUT IMPEDANCE
Master	20 dB	5.6 kΩ	OPEN	60 kΩ
Master	25 dB	20 kΩ	100 kΩ	30 kΩ
Master	32 dB	39 kΩ	100 kΩ	15 kΩ
Master	36 dB	47 kΩ	75 kΩ	9 kΩ
Slave	20 dB	51 kΩ	51 kΩ	60 kΩ
Slave	25 dB	75 kΩ	47 kΩ	30 kΩ
Slave	32 dB	100 kΩ	39 kΩ	15 kΩ
Slave	36 dB	100 kΩ	18 kΩ	9 kΩ

(1) Resistor tolerance should be 5% or better.

$$P_{OUT} = \left(\frac{R_L}{R_L + 2 \times R_f} \right)^2 \times V_p^2$$

for unclipped power

Where:
 R_f is the total series resistance including R_{OUT} and output filter resistance.
 R_L is the load resistance.
 V_p is the peak amplitude
 $V_p = 4 \times PLIMIT$ voltage if $PLIMIT < 4 \times V_p$
 P_{OUT} (10%THD) = $1.25 \times P_{OUT}$ (unclipped)

Table 3. POWER LIMIT Example

PLIMIT (V)	PLIMIT VOLTAGE (V) ⁽¹⁾	R to GND	R to GND	OUTPUT VOLTAGE (V _{rms})
24 V	DVDD	Short	Open	17.80
24 V	3.3	51 kΩ	51 kΩ	12.67
24 V	2.25	24 kΩ	51 kΩ	9.00
12 V	DVDD	Short	Open	10.33
12 V	2.25	24 kΩ	51 kΩ	9.00
12 V	1.5	18 kΩ	68 kΩ	6.30

(1) PLIMIT measurements taken with EVM gain set to 26dB and input voltage set to V_{DD}

Table 2. Recommended Input AC-Coupling Capacitors

GAIN	INPUT IMPEDANCE	INPUT CAPACITANCE	HIGH-PASS FILTER
20 dB	60 kΩ	1.5 μF	1.8 Hz
25 dB	30 kΩ	3.3 μF	1.8 Hz
32 dB	15 kΩ	5.6 μF	2.3 Hz
36 dB	9 kΩ	9.0 μF	1.8 Hz

Blanking

www.teknisi-indonesia.com

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title 030_(Reserved)

Size A Document Number Rosa_SKL-U AIO

Rev -1

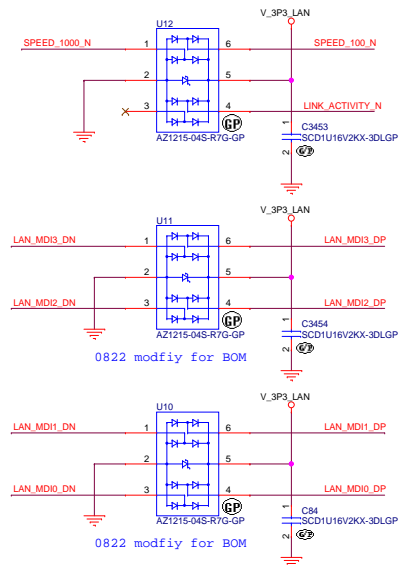
Date: Wednesday, July 01, 2015 Sheet 30 of 105

```

32 LINK_ACTIVITY_N
32 SPEED_100_N
32 SPEED_1000_N

```

ESD

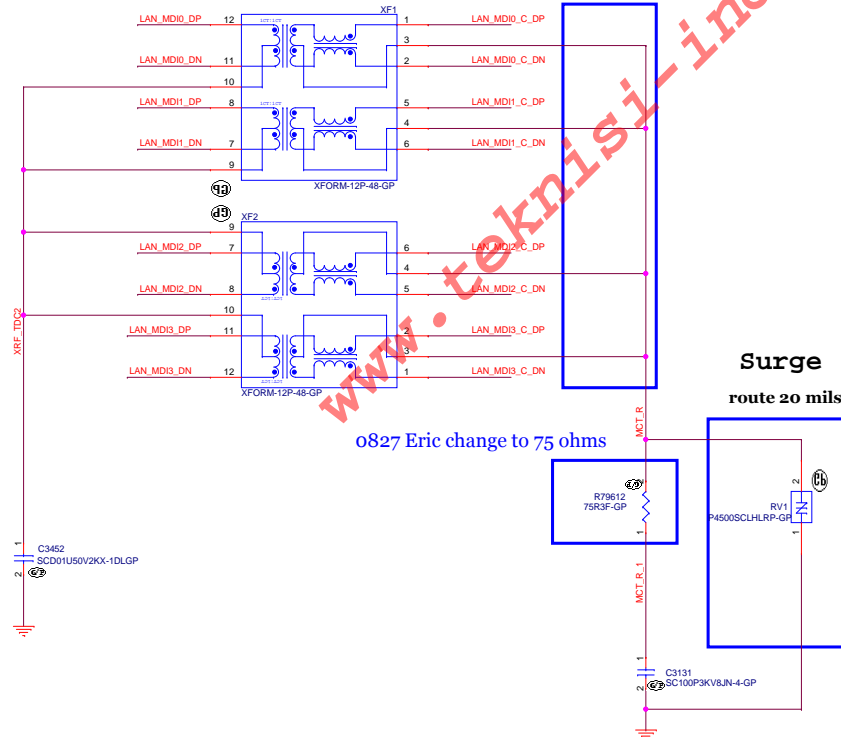


```

graph LR
    ESD[ESD] --> TRANSFORMER[TRANSFORMER]
    TRANSFORMER --> Connector[Connector]
  
```

0716 Eric modify

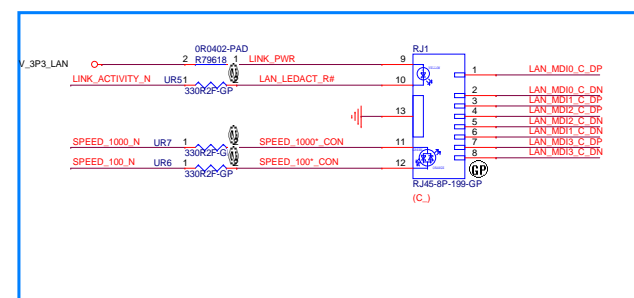
**0702 Eric modify to 1 pcs
surge SIDACTOR**



	Giga	100	10
Link	Orange	Green	Green
Act	Yellow Blink	Yellow Blink	Yellow Blink

Connector

RJ45



<Variant Name>



Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

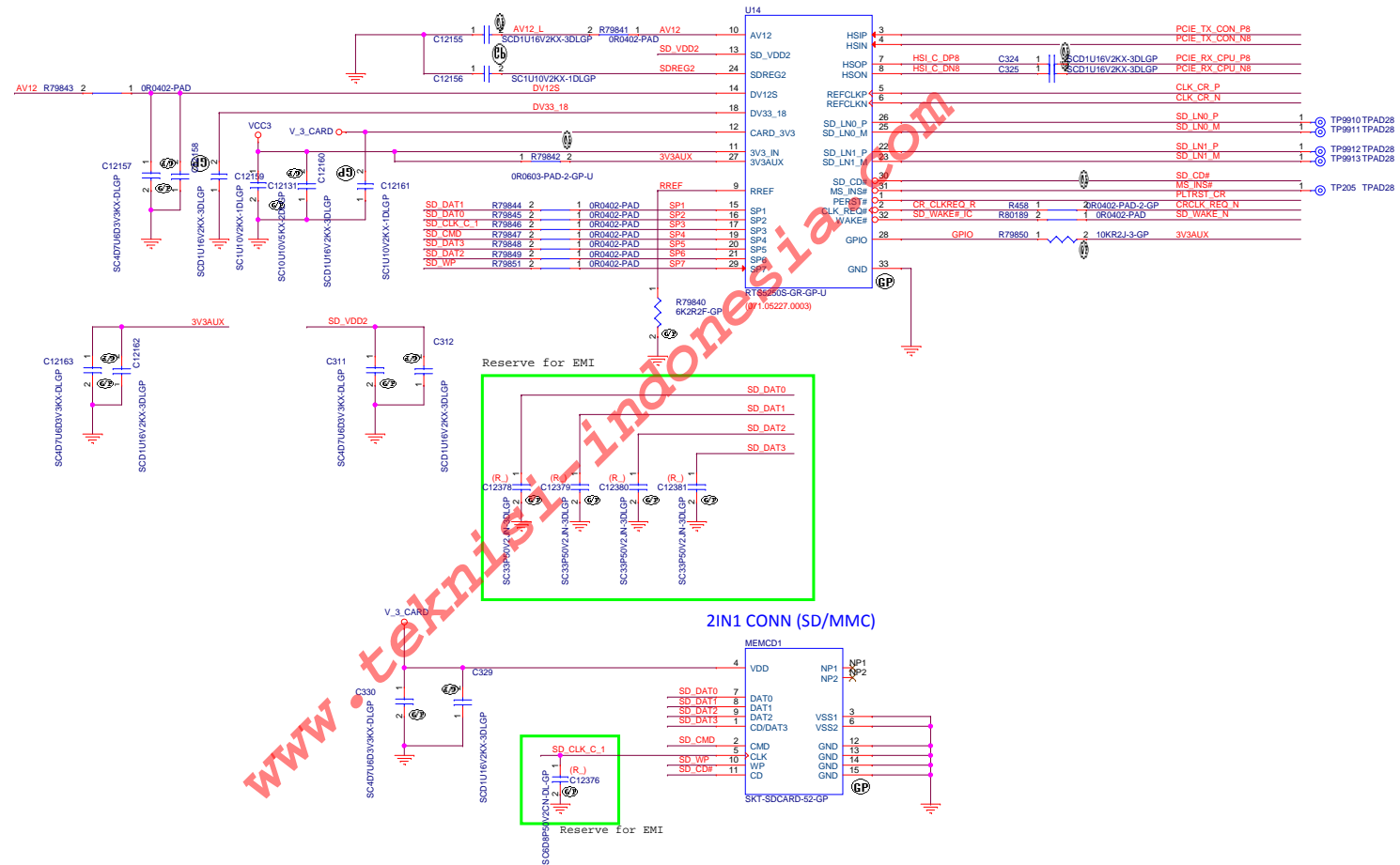
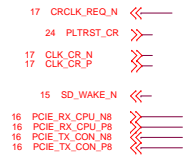
Title 032 RJ45+Transformer

Size	Document Number
C	Rosa SKL-U AIC

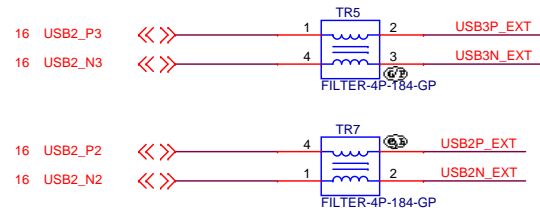
Date: Wednesday, July 01, 2015 Sheet 32 of 105

1

Card Reader

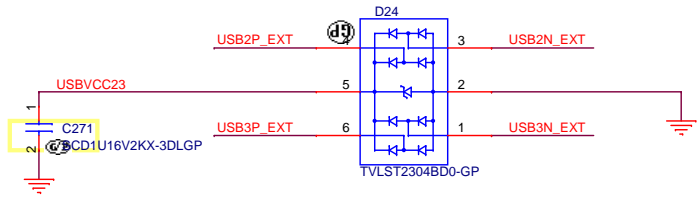


16 USB_OC#2_3 <<—
USB

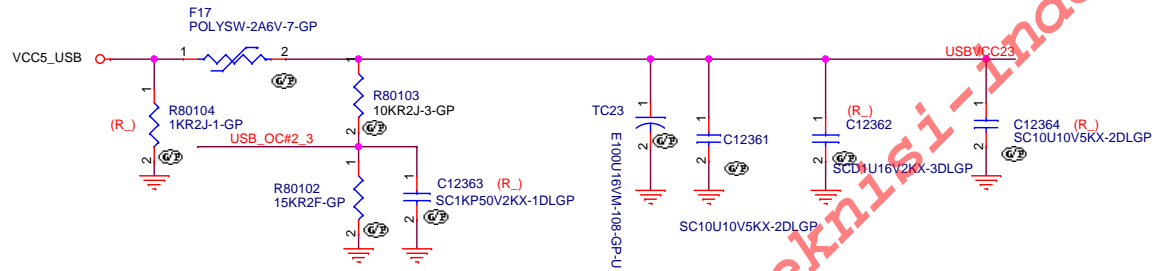
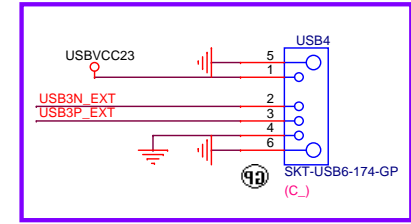
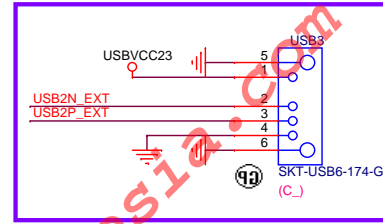


EMI

ESD



Rear USB2



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title **034_USB2.0 CONN**

Size B Document Number
Rosa_SKL-U AIO

Rev
-1

Date: Wednesday, July 01, 2015 Sheet 34 of 105

USB 3.0

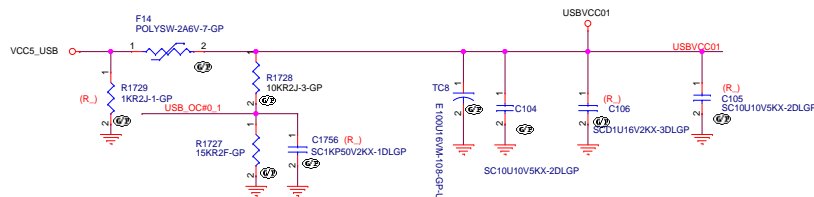
6.37 USB_OC#0_1

USB_Power...Side1

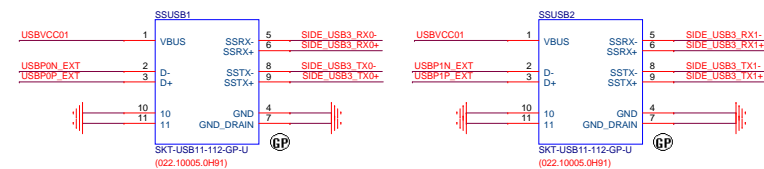
16 USB30_RX_CPU_N0
16 USB30_RX_CPU_P0
16 USB30_TX_CPU_N0
16 USB30_TX_CPU_P0
16 USB30_RX_CPU_N1
16 USB30_RX_CPU_P1
16 USB30_TX_CPU_N1
16 USB30_TX_CPU_P1

Richard Check USB Mapping

16 USB2_N0
16 USB2_P0
16.37 USB2_N1
16.37 USB2_P1
37 USB2_IN_N1
37 USB2_IN_P1



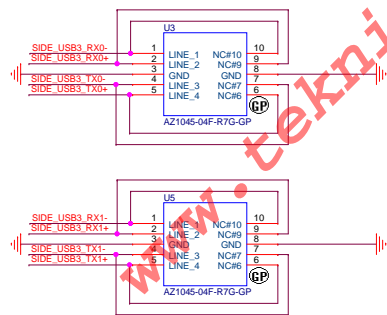
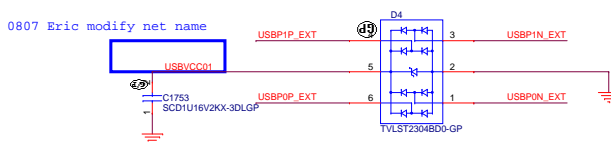
Side USB 3.0



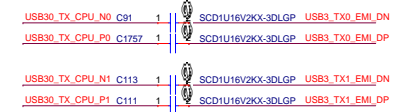
ESD

0827 Eric modify for layout

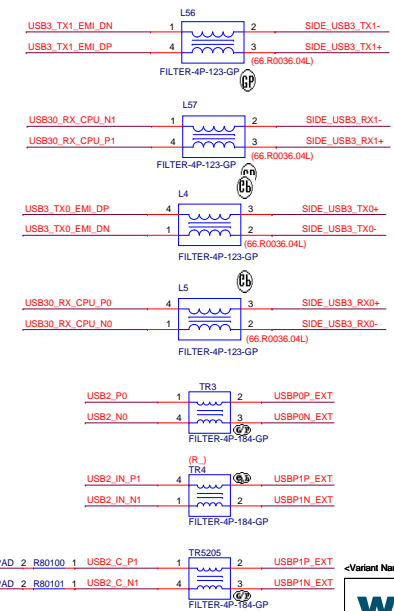
0807 Eric modify net name



EMI

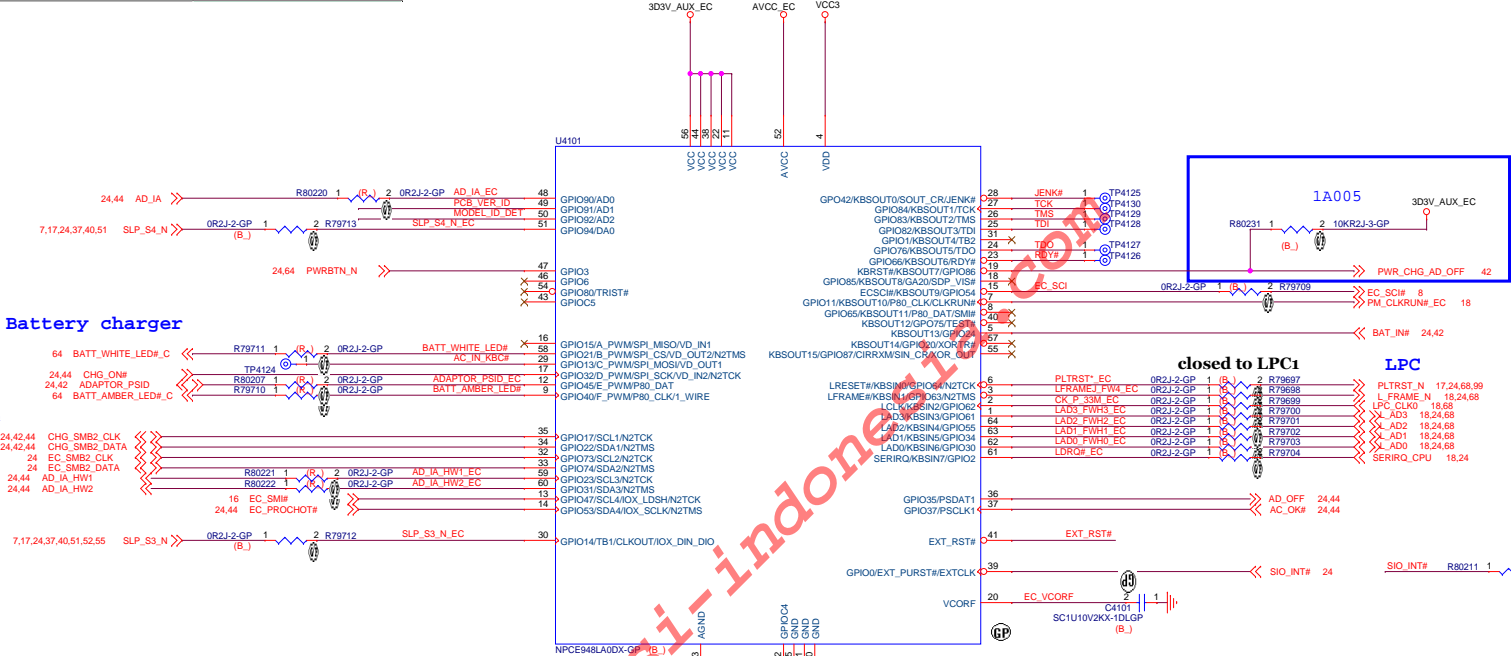


EMI

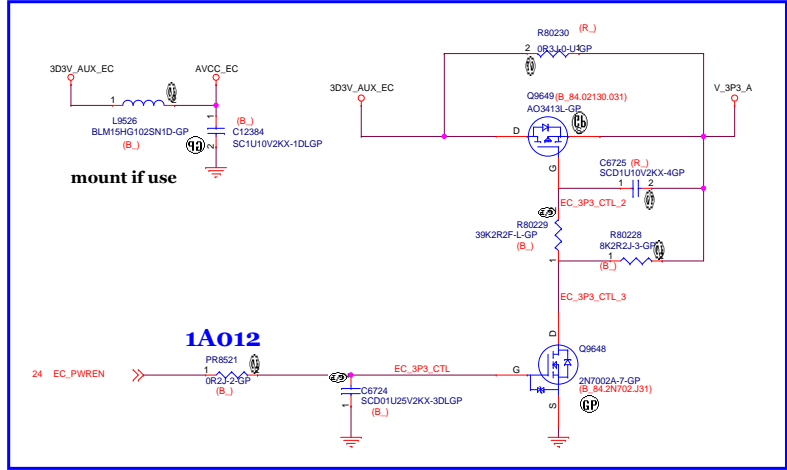
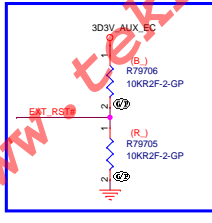
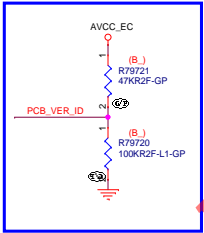
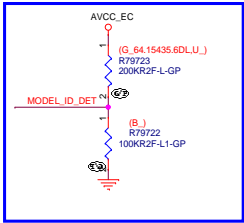
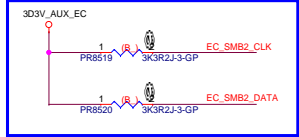


PCD_VCR_AD	Pull-Low Register	Pull-High Register	Typical Voltage
SA	100.0 K	10.0 K	3.000 V
SB	100.0 K	20.0 K	2.750 V
SC	100.0 K	33.0 K	2.481 V
-1	100.0 K	47.0 K	2.245 V

MODEL_ID_DET	Pull-Low Register	Pull-High Register	Typical Voltage
Carrizo GPU	100.0 K	10.0 K	3.000 V
Carrizo UMA	100.0 K	13.7 K	2.902 V
Braswell GPU	100.0 K	57.6 K	2.094 V
Braswell UMA	100.0 K	64.9 K	2.001 V
SKL-U GPU	100.0 K	154.0 K	1.299 V
SKL-U UMA	100.0 K	200.0 K	1.100 V



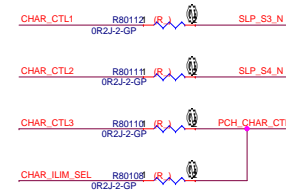
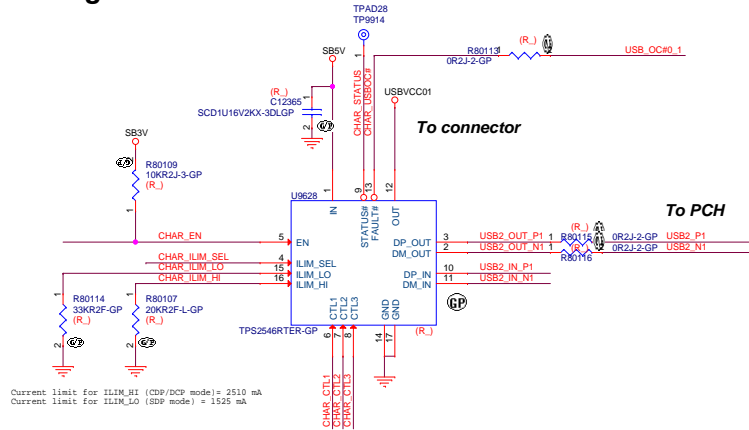
Charger SMBus PH at Charger Side



Charger IC Control



Charger IC - TI TPS2546



To PCH GPIO41

CTL1 SLP_S3#	CTL2 SLP_S4#	CTL3 GPIO41	ILIM_SEL GPIO41	Mode	State
0	0	0	0	Turn off power switch & discharge VBUS	S4/S5
0	0	1	1	DCP	S4/S5
0	1	0	0	SDP	S3
0	1	1	1	DCP with HID auto detect USB data pass through	S3
1	1	0	0	SDP	S0
1	1	1	1	CDP	S0

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title 037_USB Charger (RES)

Size C Document Number
Rosa_SKL-UAK

Rev
-1

Date: Wednesday, July 01, 2015

Sheet 37 of 105

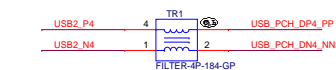
WEBCAM

15 USB2_N4
16 USB2_P4

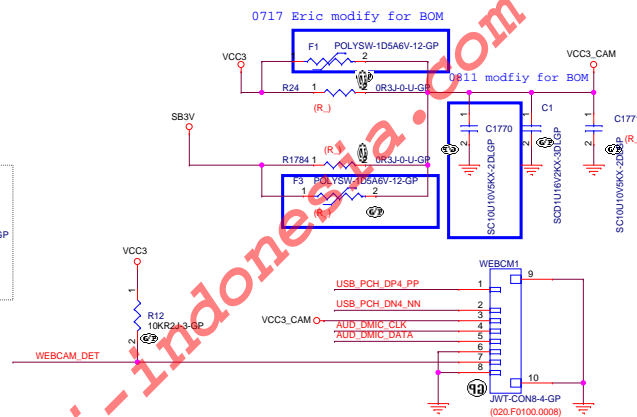
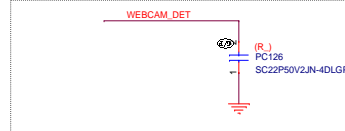
27 AUD_DMIC_CLK
27 AUD_DMIC_DATA

24 WEBCAM_DET

WEBCAM



FOR EMI



<Variant Name>

wlstron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title **038_WEBCAM**

Size C Document Number
Rosa_SKL-U-AR0

Rev
-1

Date: Wednesday, July 01, 2015 Sheet 38 of 105

Blanking

www.teknisi-indonesia.com

<Variant Name>

wistron

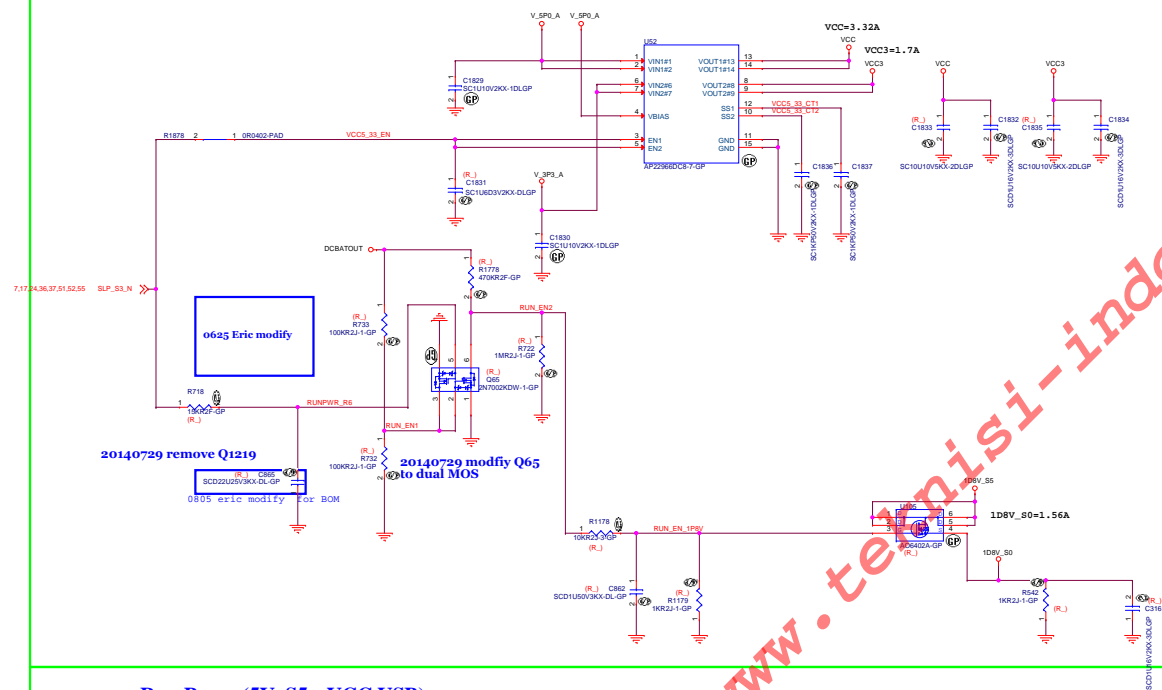
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title 039_(Reserved)

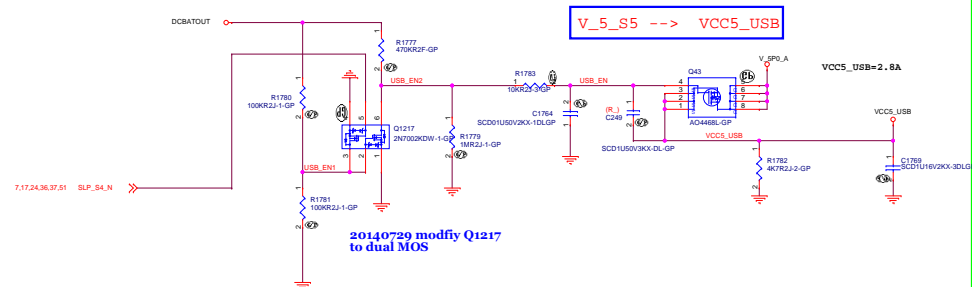
Size Document Number
A Rosa_SKL-U AIO

Rev
-1

Date: Wednesday, July 01, 2015 Sheet 39 of 105

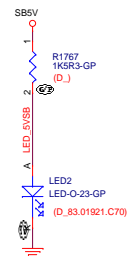
[illegible]

V_5_S5 --> VCC5_US



VCC5SB LED

0811 Eric delete 5V always LED



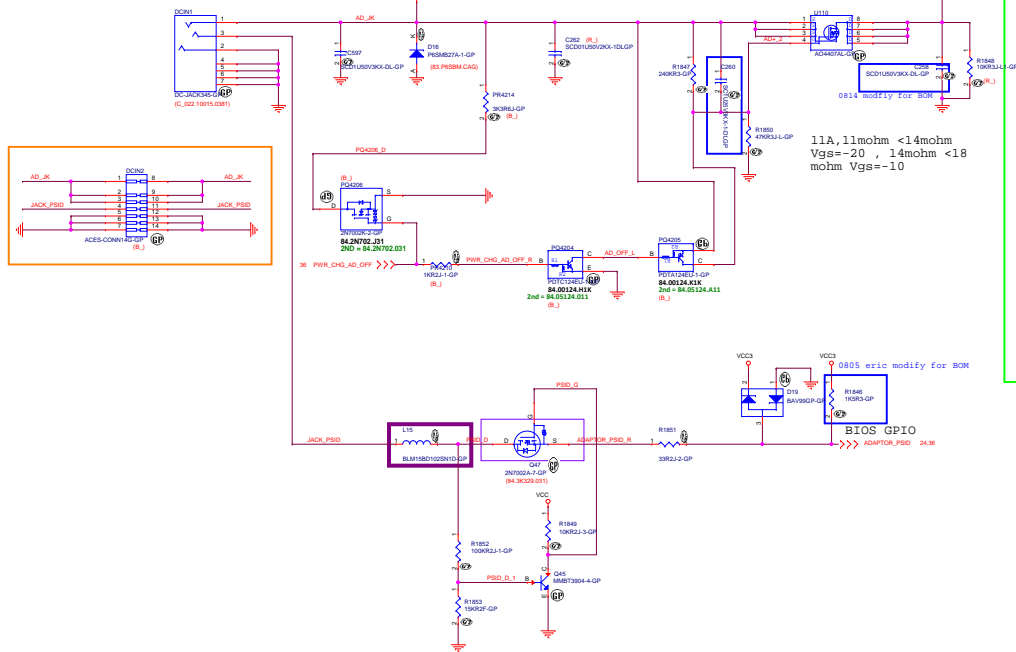
DCIN

For layout top and bottom the same
U33

R981 R982 R983
R1718

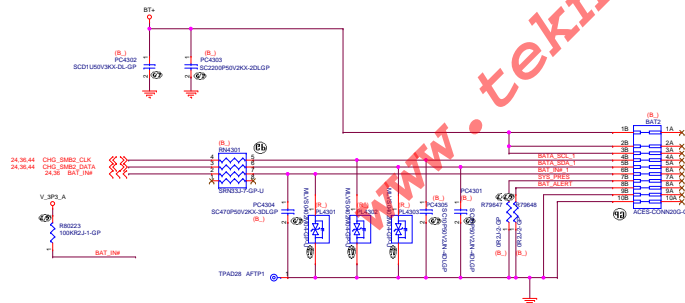
Adaptor in to generate DCBATOUT

DC in



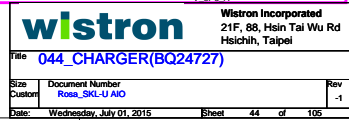
0721 delete power limit circuit

BATTERY CONNECTOR

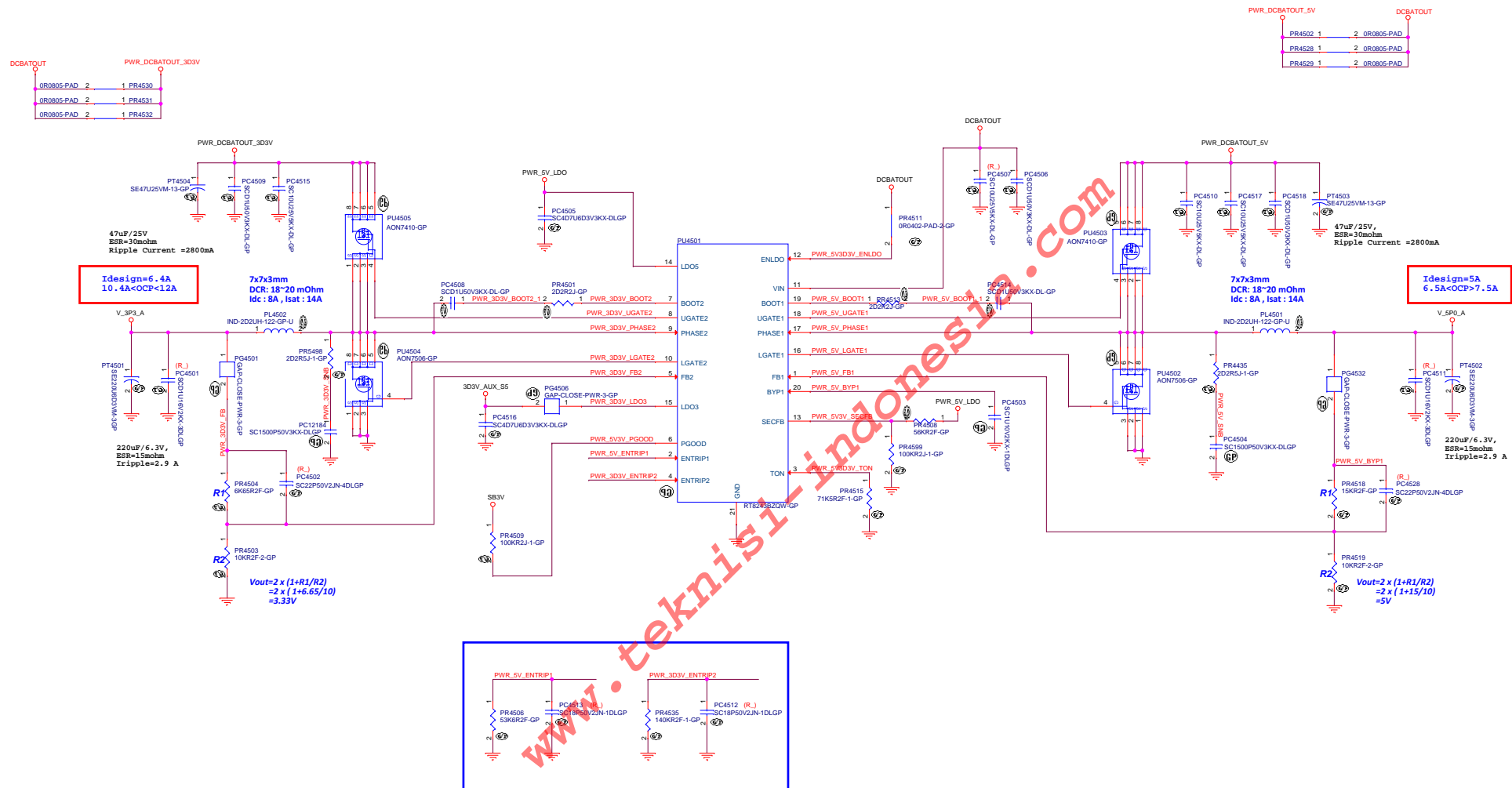


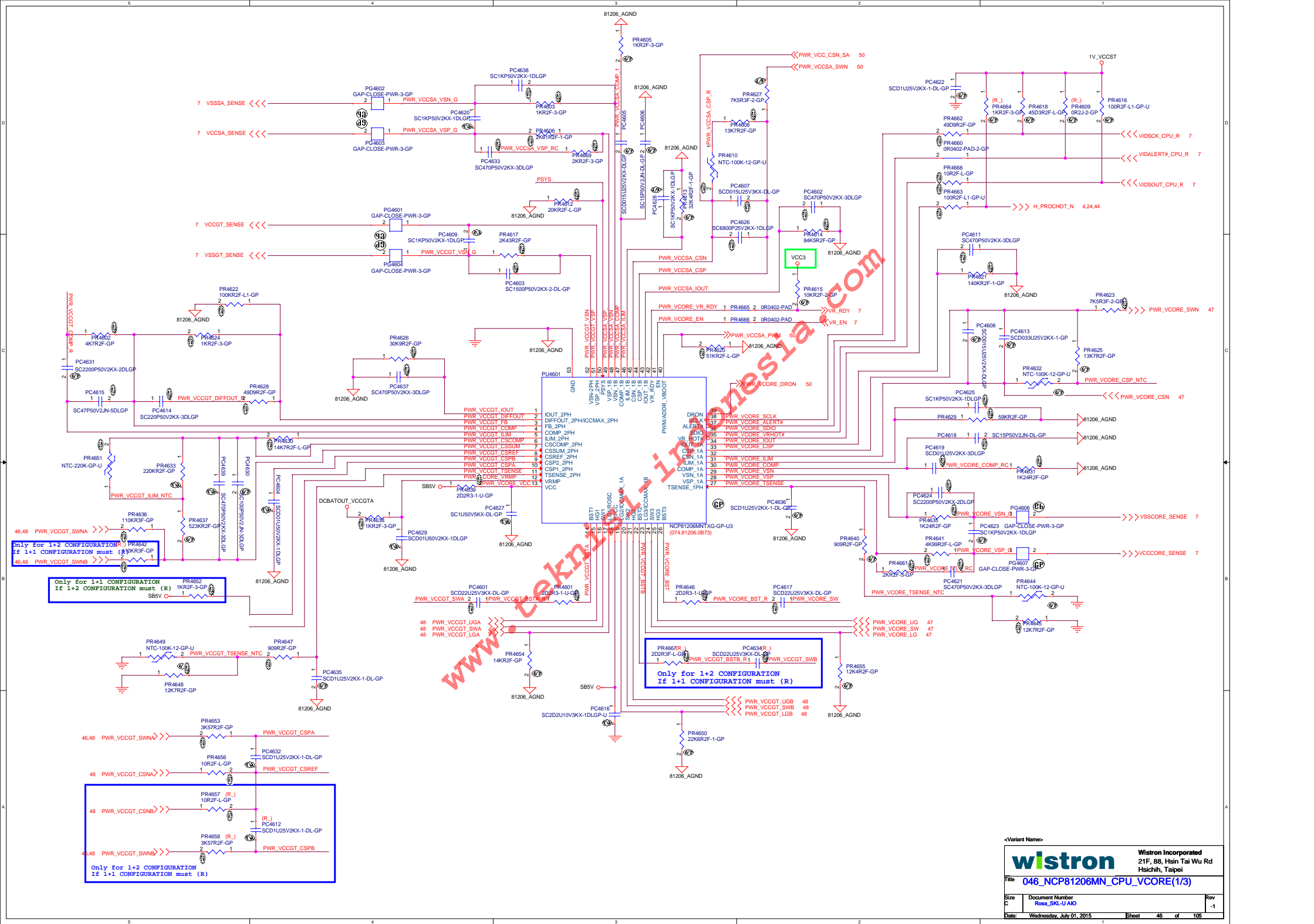
Blanking

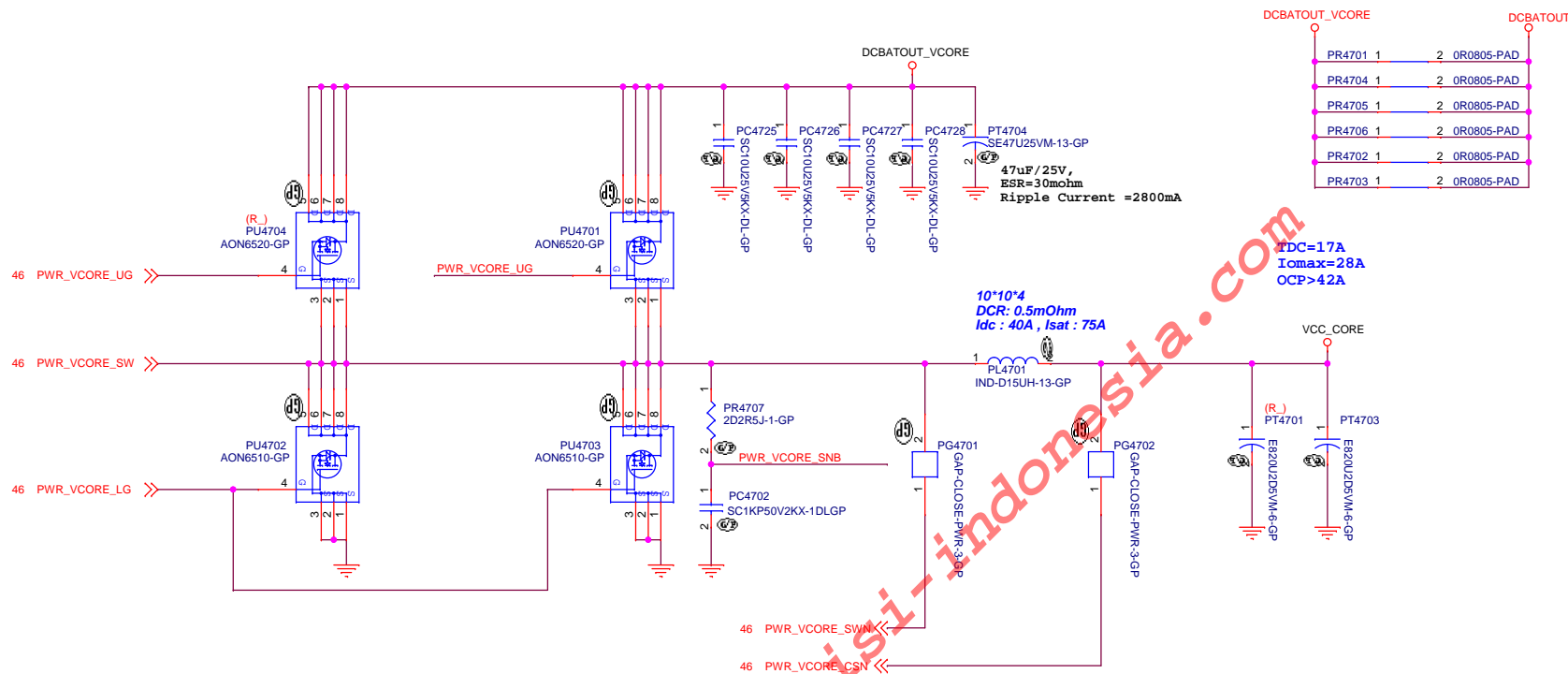
www.teknisi-indonesia.com



```
SSID = PWR.Plane.Regulator_5V/3D3V
```







<Variant Name>

wistron

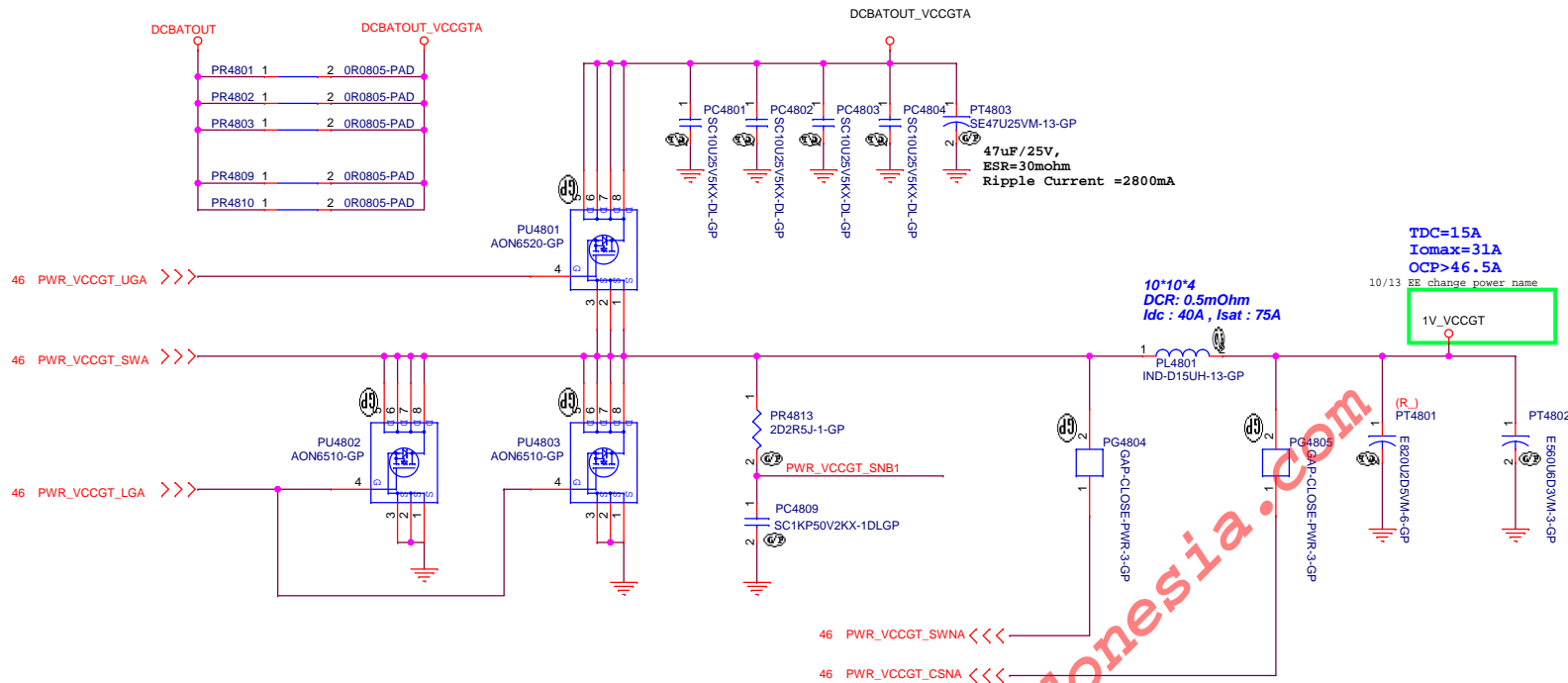
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title 047_NCP81206MN_CPU_VCORE(2/3)

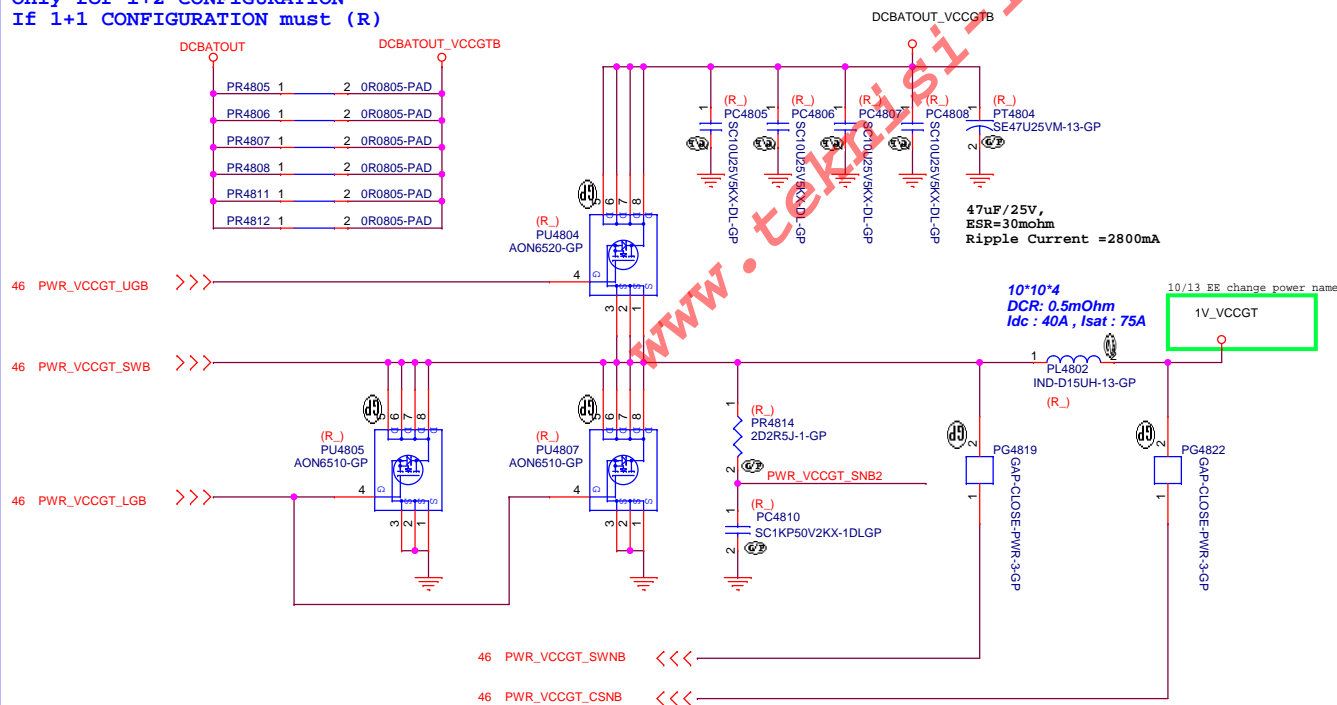
Size A3 Document Number Rosa_SKL-U AIO

Rev -1

Date: Wednesday, July 01, 2015 Sheet 47 of 105



Only for 1+2 CONFIGURATION
If 1+1 CONFIGURATION must (R)



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title 048_NCP81206MN_CPU_VCCGT(3/3)

Size A3 Document Number Rosa_SKL-U AIO

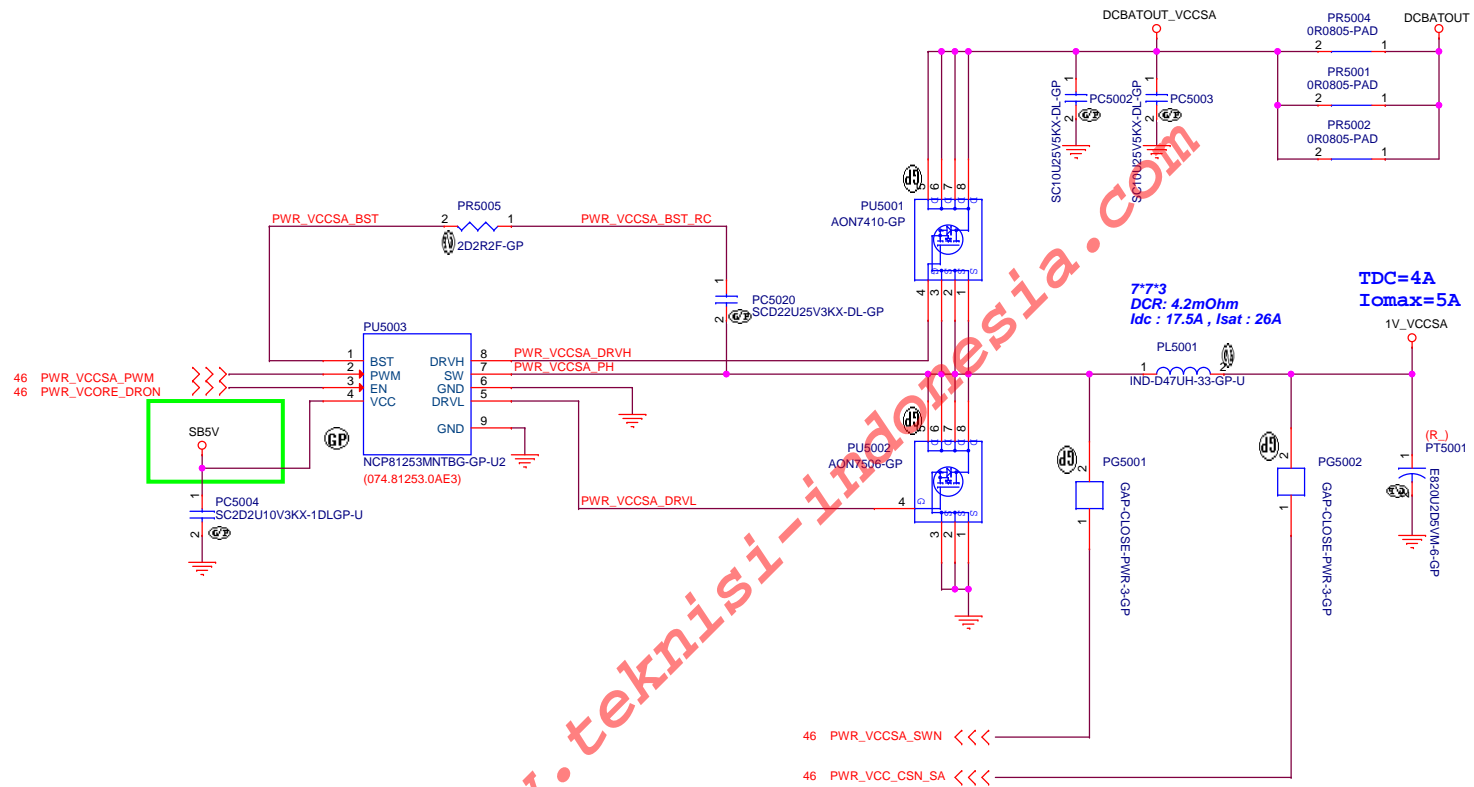
Rev -1

Date: Wednesday, July 01, 2015

Sheet 48 of 105

Blanking

www.teknisi-indonesia.com



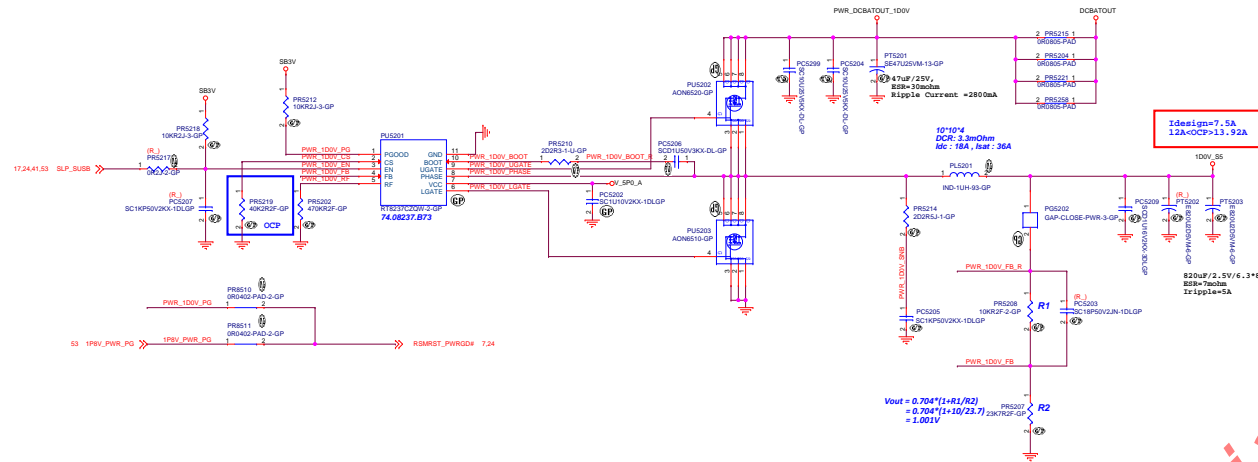
<Variant Name>

wistron

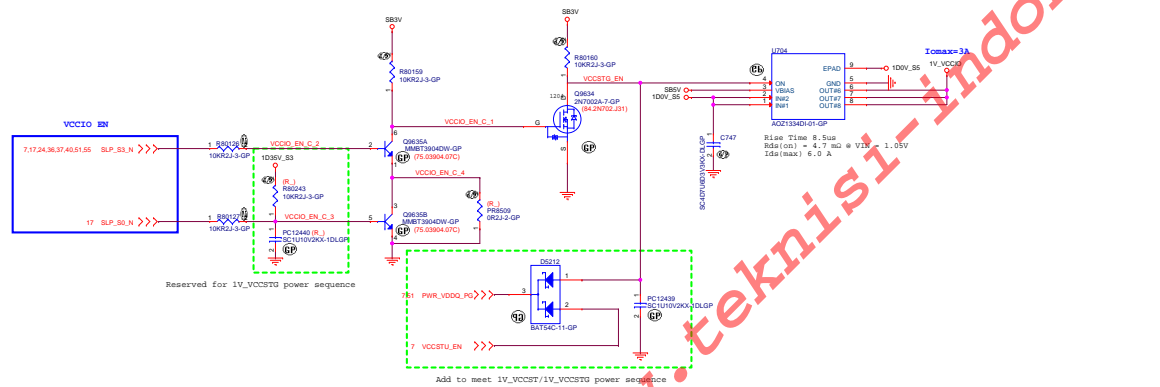
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title 050_NCP81253MN_CPU_VCCSA

Size A3	Document Number Rosa_SKL-U AIO	Rev -1
Date Wednesday, July 01, 2015	Sheet 50 of 105	

RT8237 for 1D0V

Load Switch for VCCIO



VCCPRIM_CORE Connects to 1D0V

 $I_{\text{max}} = 2.57 \text{ A}$

Connection moved to page 7

Blanking

www.teknisi-indonesia.com

SSID = Scalar

Audio Out

L200-002

L200-002

L200-002

L200-002

L200-002

L200-002

L200-002

L200-002

L200-002

L200-002

L200-002

L200-002

L200-002

L200-002

L200-002

L200-002

L200-002

L200-002

L200-002

L200-002

L200-002

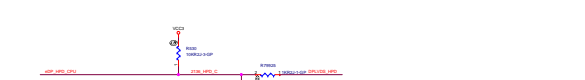
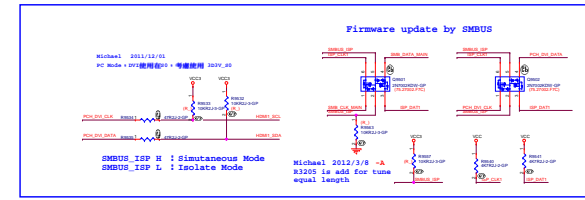
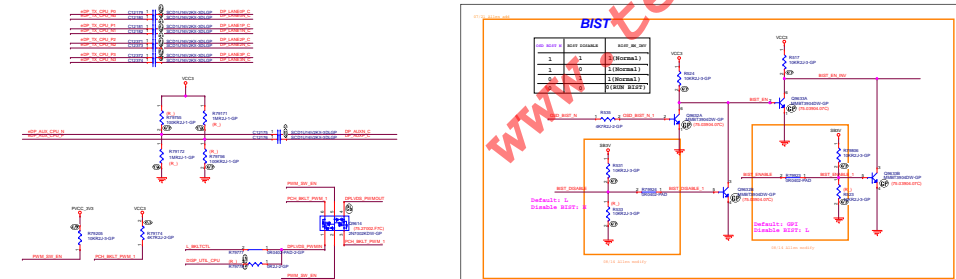
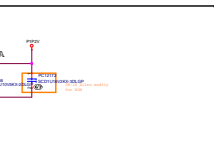
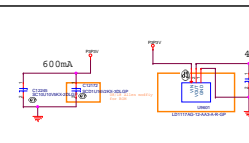
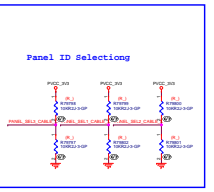
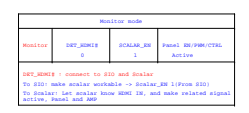
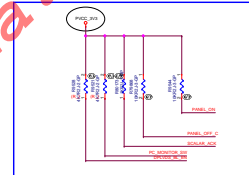
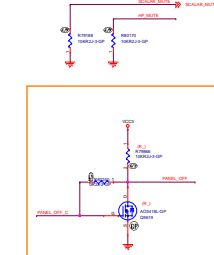
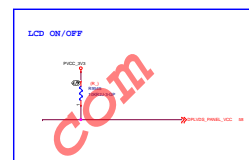
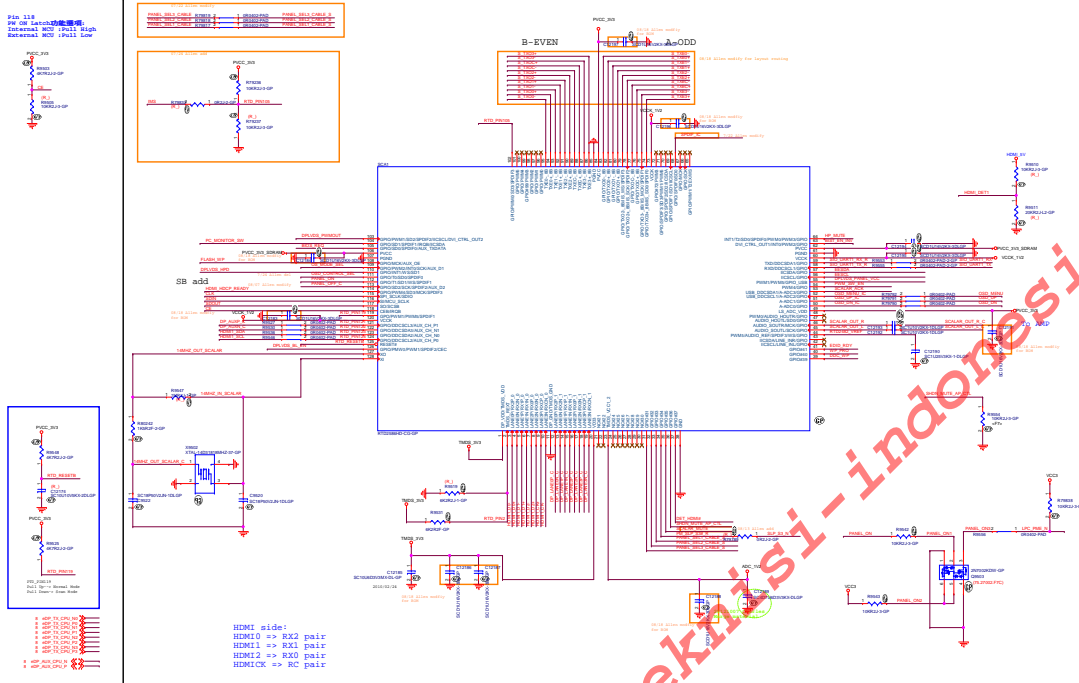
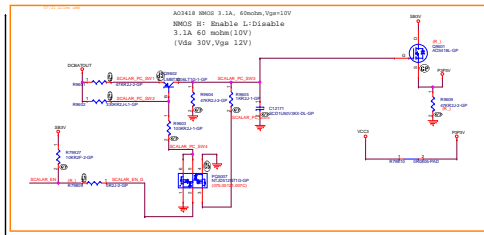
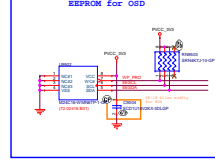
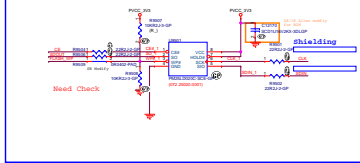
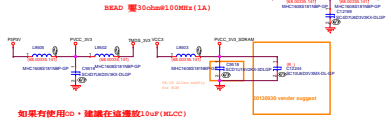
L200-002

L200-002

L200-002

L200-002

L200-002



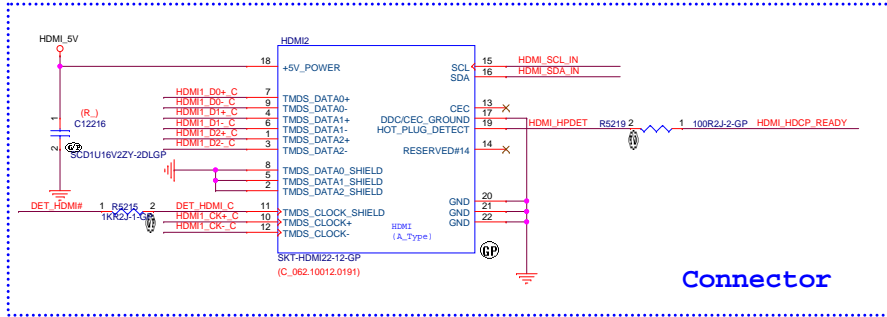
HDMI-IN

HDMI

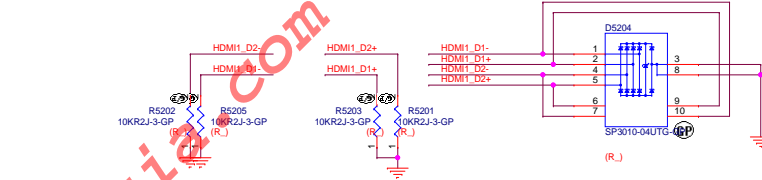
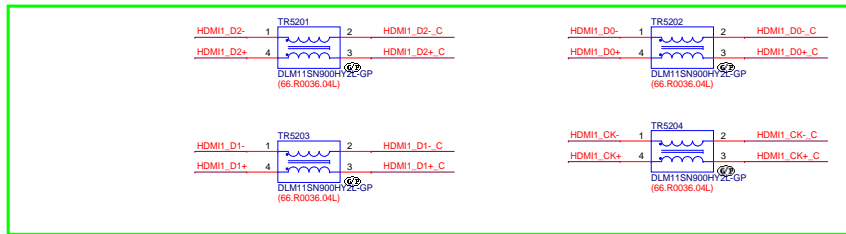
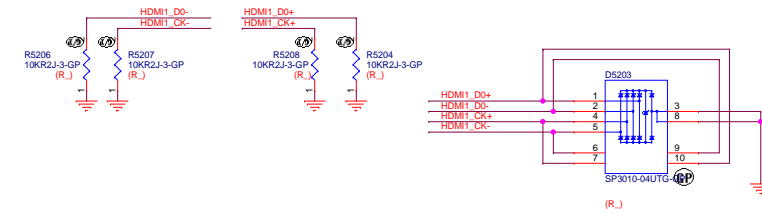
55 HDMI1_D2+ <<<
55 HDMI1_D2- <<<
55 HDMI1_D1+ <<<
55 HDMI1_D1- <<<
55 HDMI1_D0+ <<<
55 HDMI1_D0- <<<
55 HDMI1_CK+ <<<
55 HDMI1_CK- <<<

24.55 DET_HDMI# <<<

55 DDC_WP <<<
55 HDMI1_SDA <<<
55 HDMI1_SCL <<<
55 HDMI_HDCP_READY <<<

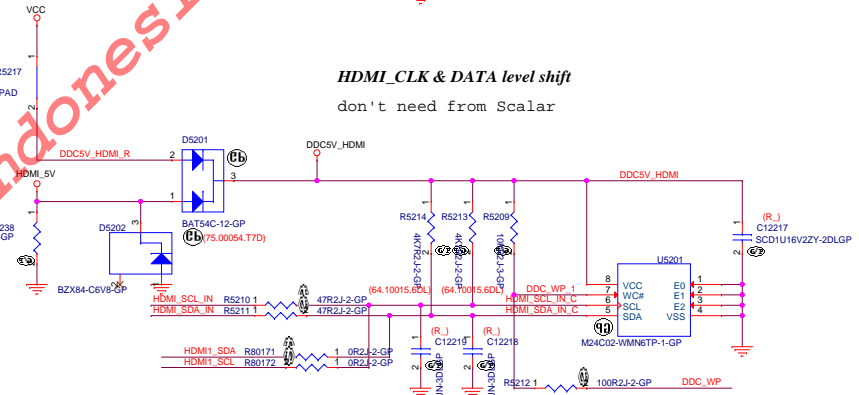
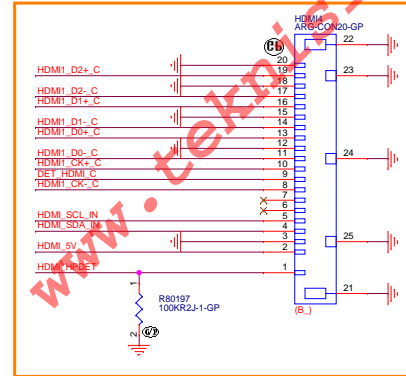
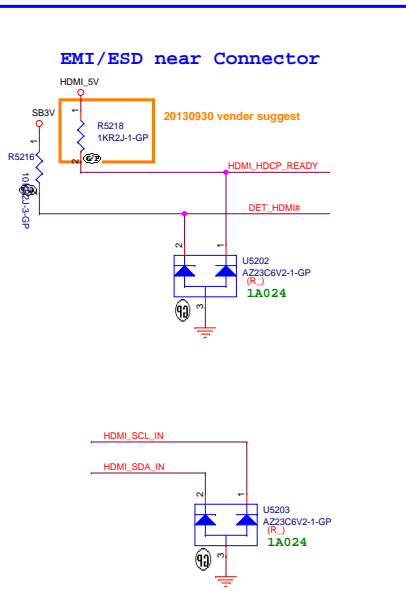


EMI/ESD near Connector



HDMI_CLK & DATA level shift

don't need from Scalar



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

File 056_HDMI_IN

Size C Document Number
Rosa_SKL-UAK

Rev -1

Date: Wednesday, July 01, 2015 Sheet 56 of 105

HDMI

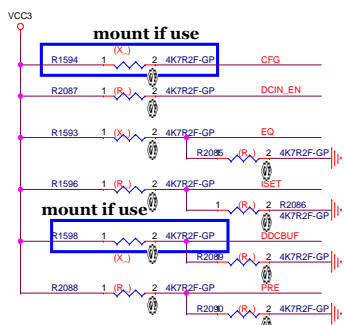
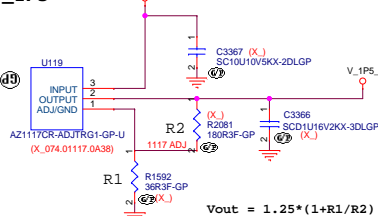
Need to add diode!!!

8 HDMI1_DATA_CPU_P0
8 HDMI1_DATA_CPU_N0
8 HDMI1_DATA_CPU_P1
8 HDMI1_DATA_CPU_N1
8 HDMI1_DATA_CPU_P2
8 HDMI1_DATA_CPU_N2
8 HDMI1_DATA_CPU_P3
8 HDMI1_DATA_CPU_N3

8 HDMI1_CTRL_CLK_CPU
8 HDMI1_CTRL_DATA_CPU
8 HDMI1_OUT_HPD
24 EC_HDMI_PD_N

Reserved for HDMI re-Driver

V_1P5

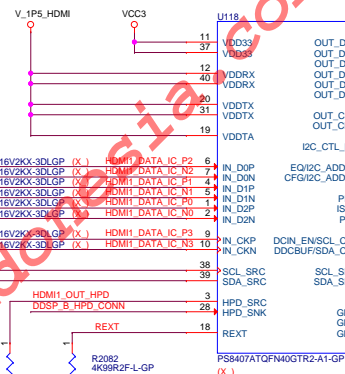
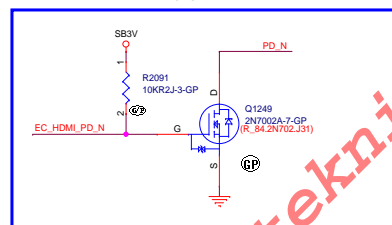
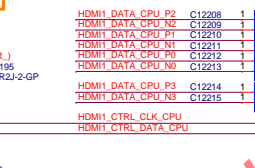
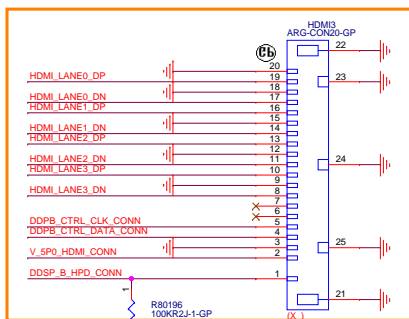


Near Pin 19

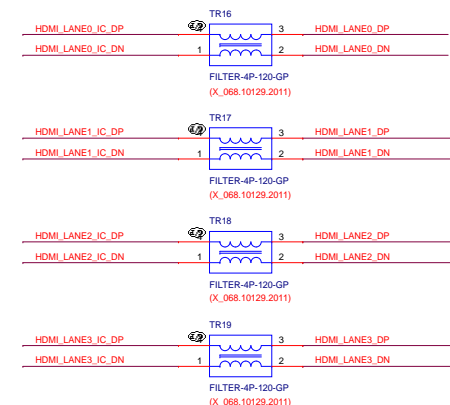
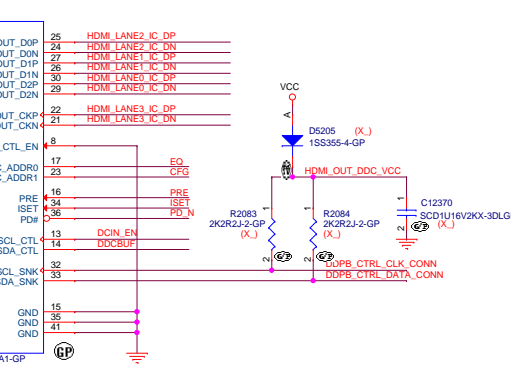
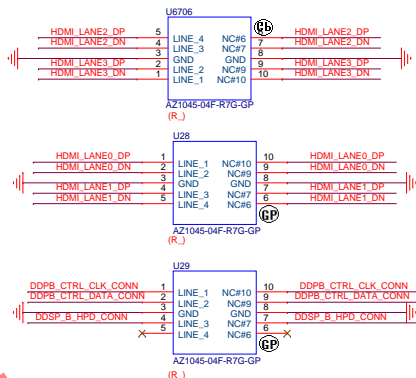
Near Pin 20, 31

Near Pin 12, 40

Near Pin 11, 37



ESD



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

File 057_HDMI_OUT

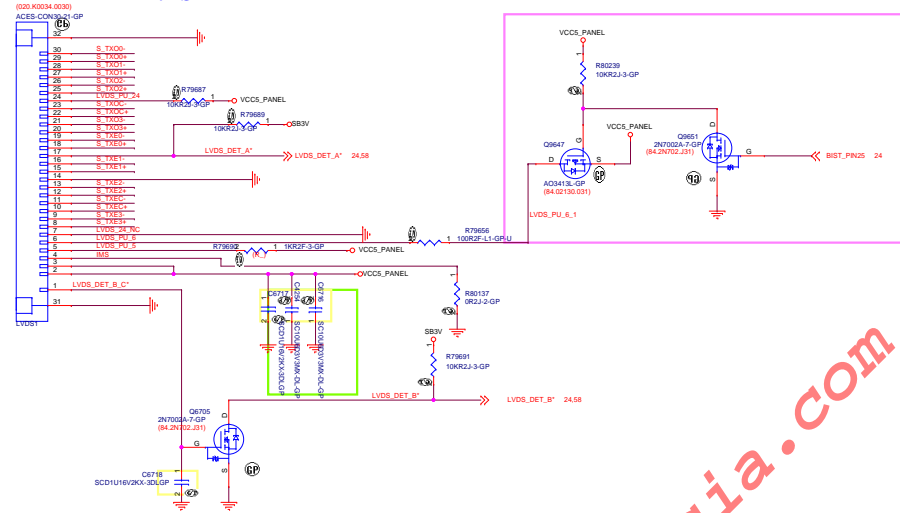
Size C Document Number Rosa_SKL-U40

Date: Wednesday, July 01, 2015

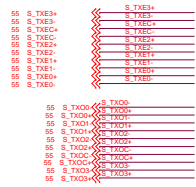
Sheet 57 of 105

Rev -1

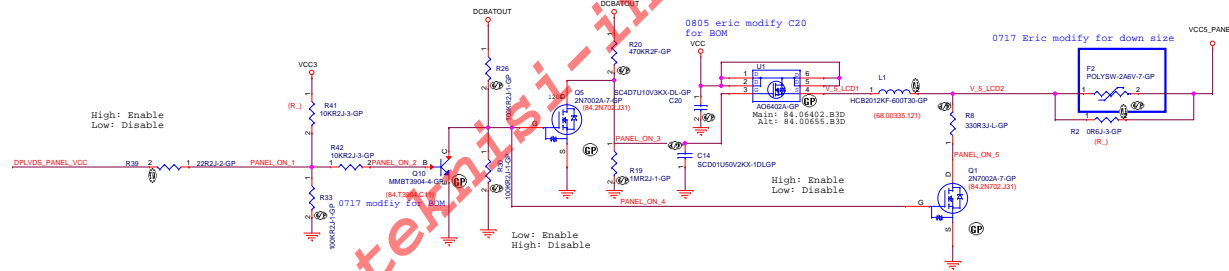
LVDS1



From RTD2136S to LVDS



GPIO



24.05 PANEL_SEL1_CABLE
24.05 PANEL_SEL2_CABLE
24.05 PANEL_SEL3_CABLE

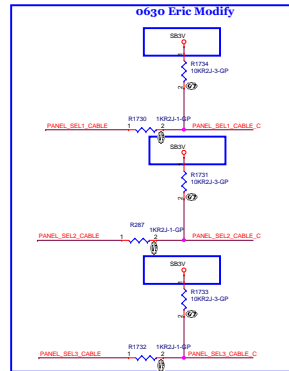
24.59 SIO_LVDS_BL_ADJ >> SIO_LVDS_BL_ADJ

55 DPLVDS_PWMOUT >> DPLVDS_PWMOUT

24.59 DPLVDS_BL_EN >> DPLVDS_BL_EN

24 SIO_SMDATA
24 SIO_SMDATA

Cable detection			
PANEL_SEL1	PANEL_SEL2	PANEL_SEL3	Status
1	1	1	Panel unplug
X	X	X	Panel plug

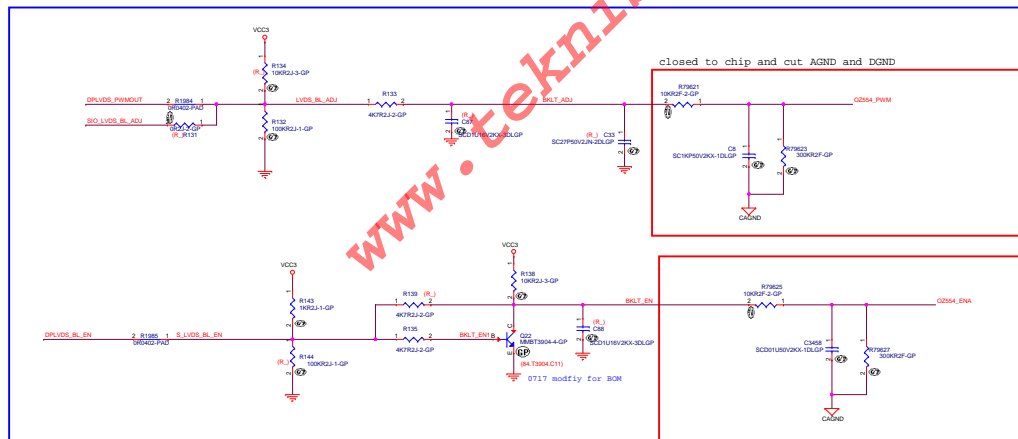


1A014

Cable Spec			
23.8"Panel Model	PANEL_SEL1	PANEL_SEL2	PANEL_SEL3
LG	1	0	0
BOE	1	1	0
AUO	1	0	1
19.5"Panel Model	PANEL_SEL1	PANEL_SEL2	PANEL_SEL3
AUO	0	1	0
LG	0	0	1
21.5"Panel Model	PANEL_SEL1	PANEL_SEL2	PANEL_SEL3
LG	0	0	0
Sansung	0	1	1

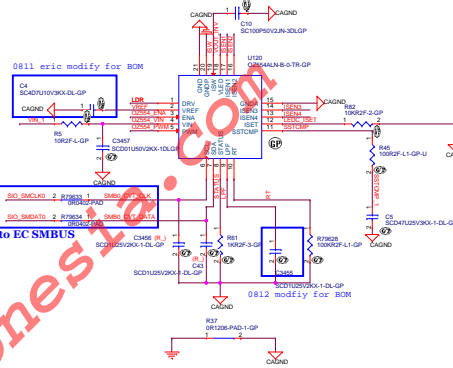
Vout(pin number of CONV1)

24.59 SIO_LVDS_BL_ADJ >> SIO_LVDS_BL_ADJ



0703 Eric modify

1st source: 83.3K010.CSM
2nd source: 83.3K010.ASM



1-008

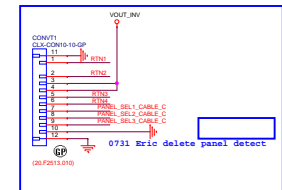
JEN1 2 B1 1 RTN1

JEN2 2 B1 1 RTN2

JEN3 2 B1 1 RTN3

JEN4 2 B1 1 RTN4

0703 Eric modify

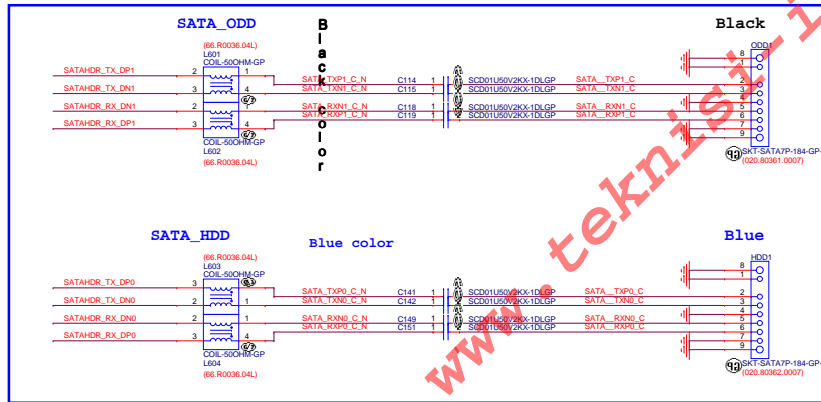
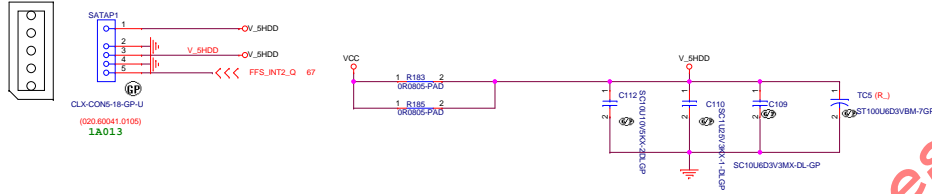


SATA

- 16 SATAHDR_RX_DP0
- 16 SATAHDR_RX_DN0
- 16 SATAHDR_TX_DN0
- 16 SATAHDR_TX_DP0
- 16 SATAHDR_RX_DP1
- 16 SATAHDR_RX_DN1
- 16 SATAHDR_TX_DN1
- 16 SATAHDR_TX_DP1

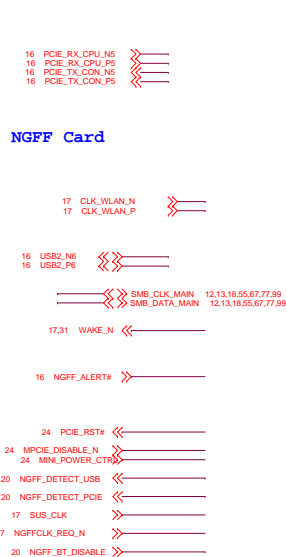
SATA

Layout: Please put them together

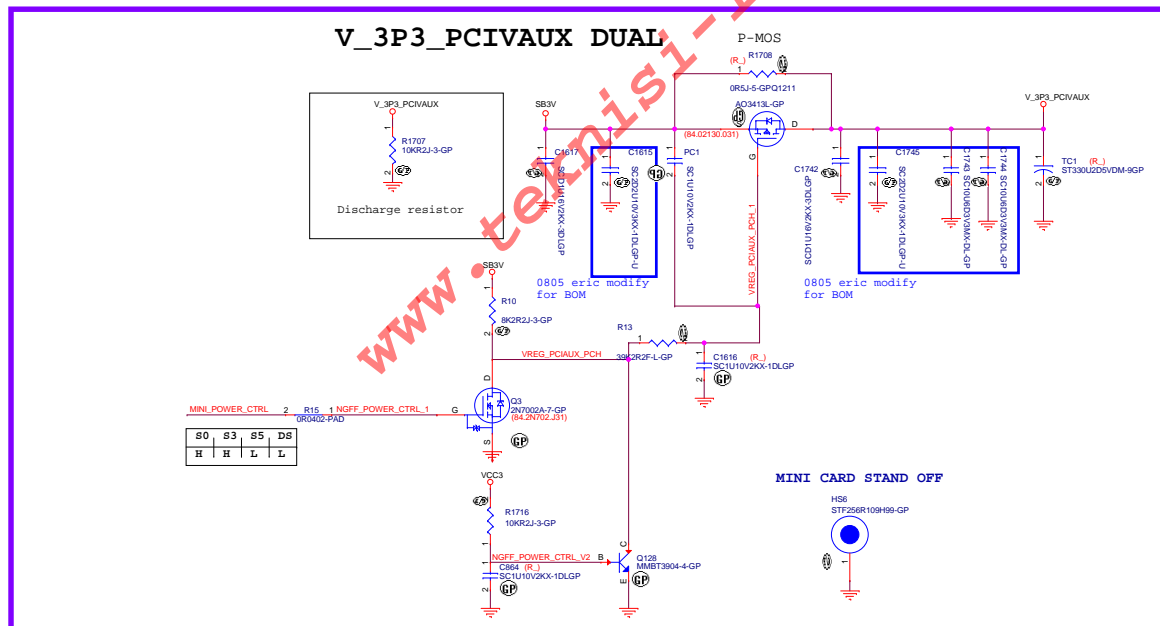
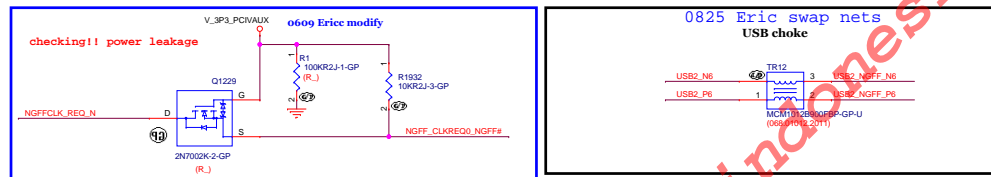
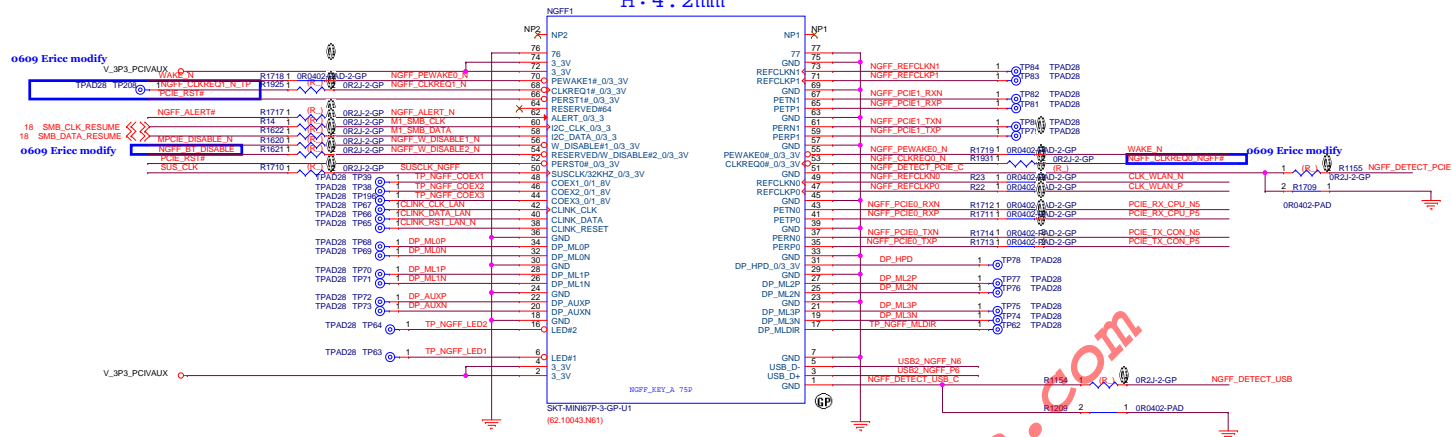


NGFF(A Key)

H: 4.2mm



NGFF Card



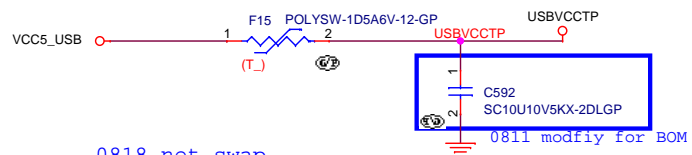
<Variant Name>

USB TOUCH PANEL

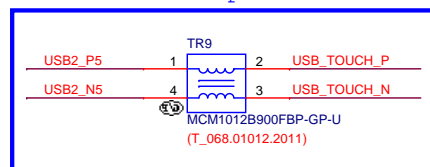
24 TP_DET <<—

16 USB2_N5 <<<<
16 USB2_P5 <<<<

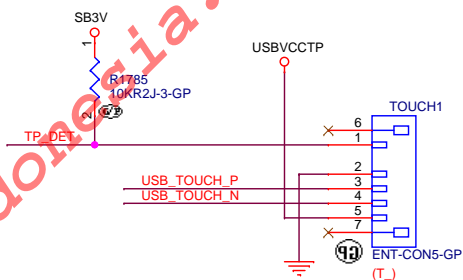
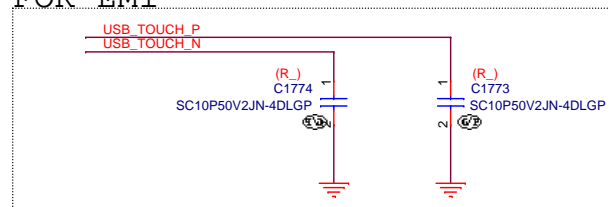
TOUCH PANEL



0818 net swap



FOR EMI



<Variant Name>

wistron**Wistron Incorporated**
21F, 88, Hsin Tai Wu Rd
Hsichih, TaipeiTitle **062_TOUCH**Size B Document Number
Rosa_SKL-U AIORev
-1

Date: Wednesday, July 01, 2015

Sheet 62 of 105

Blanking

www.teknisi-indonesia.com

<Variant Name>



Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title **063_(Reserved)**

Size A4	Document Number Rosa_SKL-U AIO	Rev -1
------------	---	-----------

Date: Wednesday, July 01, 2015 Sheet 63 of 105

Power Button/Reset

24,36 PWRBTN_N << PWRBTN_N

TO SIO

HD_LED

16 SATA_LED_N >>

24 SIO_HDD_LED >>

24 SIO_YELLOW >>

24 SIO_GREEN >>

24 SIO_GREEN_PWM <<

36 BATT_AMBER_LED_C >>

36 BATT_WHITE_LED_C >>

OSD

18,24,55 OSD_MENU << OSD_MENU

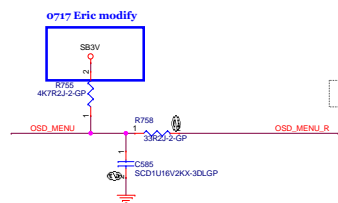
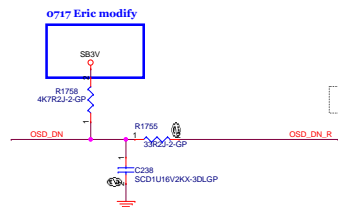
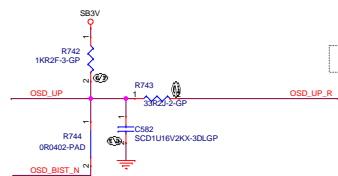
20,55 OSD_UP << OSD_UP

20,55 OSD_DN << OSD_DN

55 OSD_BIST_N << OSD_BIST_N

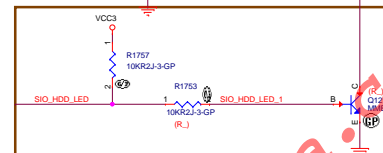
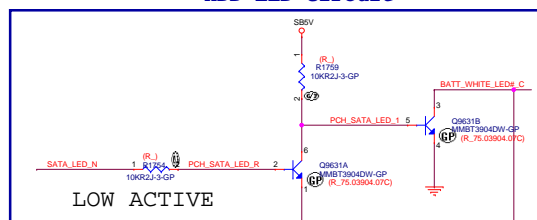
16 PWRON_DET_N << PWRON_DET_N

OSD Buttons

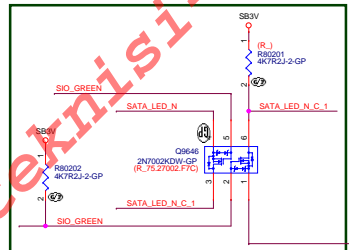


	Function
BTN1	UP
BTN2	DOWN
BTN3	Panel Off

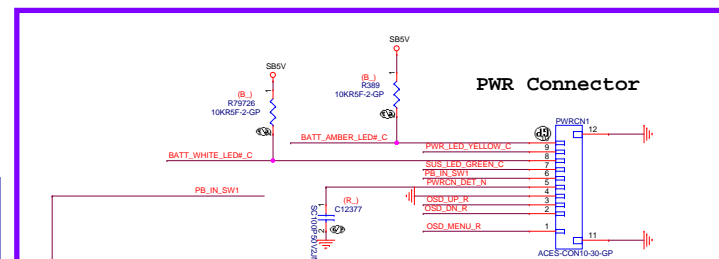
HDD LED Circuit



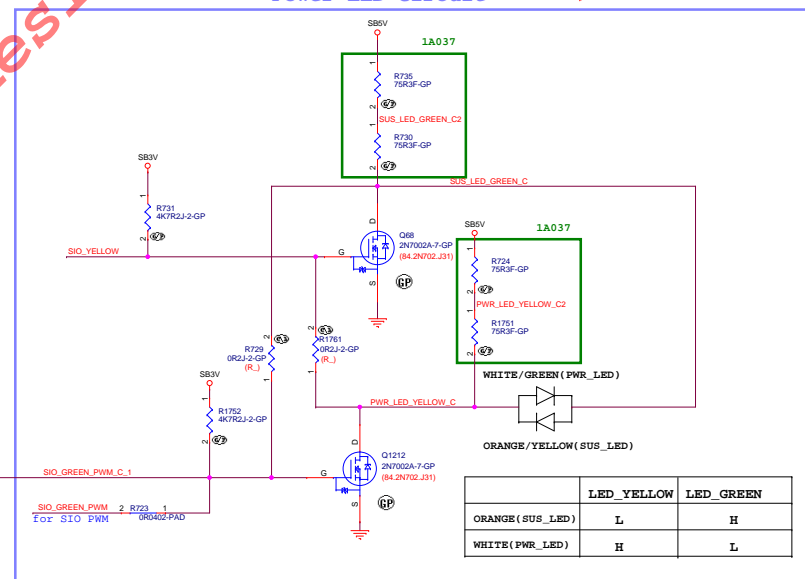
Reserve for HDD LED Control on Power LED



PWR Connector



Power LED Circuit



	LED_YELLOW	LED_GREEN
ORANGE (SUS_LED)	L	H
WHITE (PWR_LED)	H	L

~Variant Names

Blanking

www.teknisi-indonesia.com

<Variant Name>



Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title **065_(Reserved)**

Size A4	Document Number Rosa_SKL-U AIO	Rev -1
------------	--	-----------

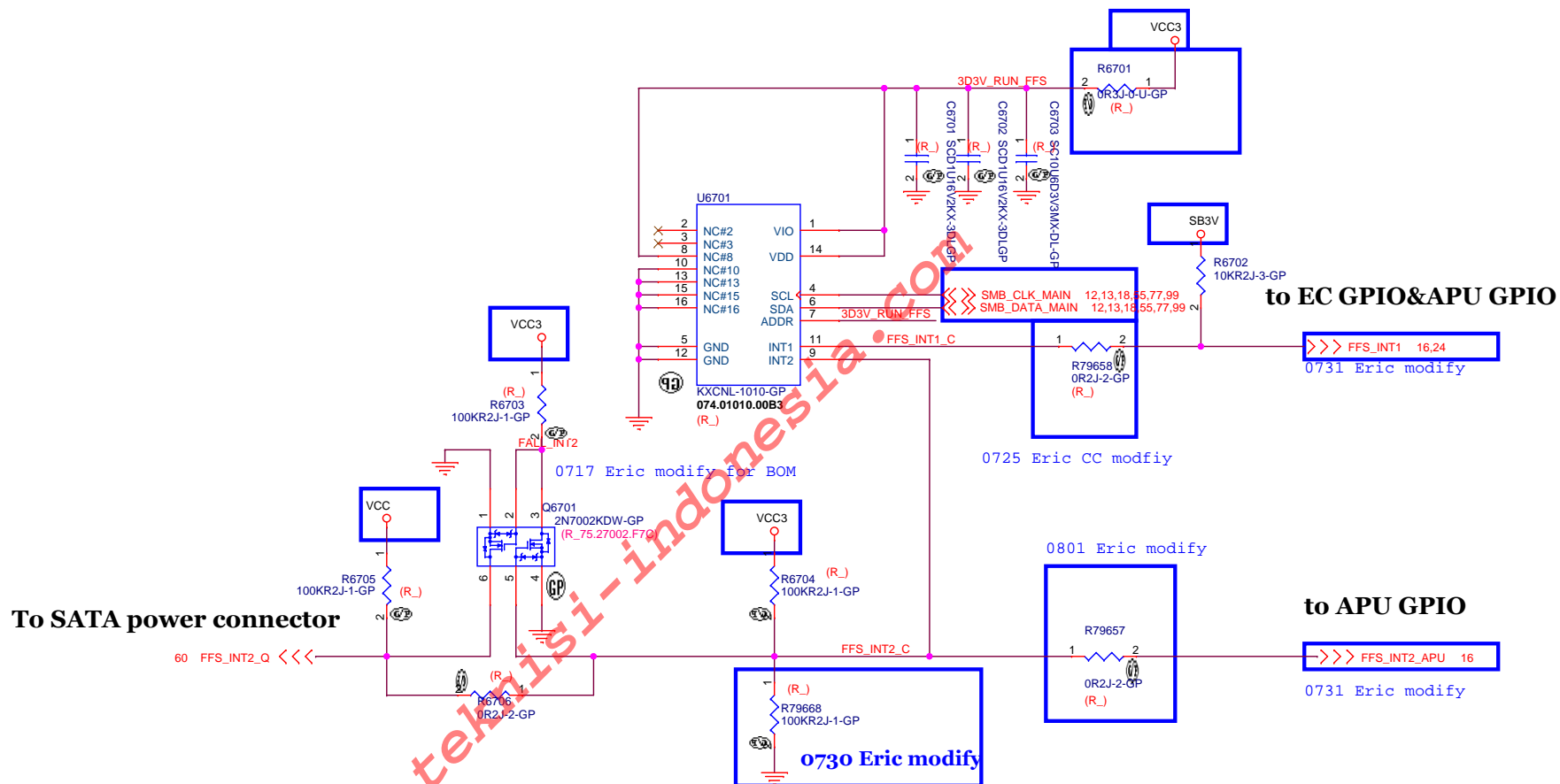
Date: Wednesday, July 01, 2015 Sheet 65 of 105

Blanking

www.teknisi-indonesia.com

Free Fall Sensor

0716 modfiy from PLANO



Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Note

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title **067_FFS(NEW)**

Size	Document Number	Rev
B	Rosa_SKL-U AIO	-1

Date: Wednesday, July 01, 2015 Sheet 67 of 105

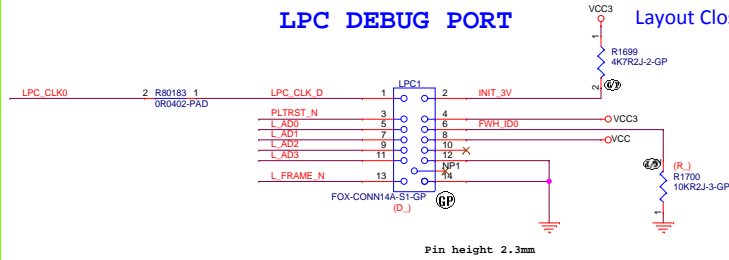
LPC DEBUG PORT

18,24,36 L_AD0
18,24,36 L_AD1
18,24,36 L_AD2
18,24,36 L_AD3
18,24,36 L_FRAME_N
17,24,36,99 PLTRST_N
18,36 LPC_CLK0

LPC DEBUG PORT

Layout Close SIO

LPC



Follow Eagle

www.teknisi-indonesia.com

<Variant Name>

wlstron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title 068_DEBUG/HDT(new)

Size Document Number
C Rosa_SKL-U ARD

Rev
-1

Date: Wednesday, July 01, 2015 Sheet 68 of 105

Blanking

www.teknisi-indonesia.com

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title **069_(Reserved)**

Size
A Document Number
Rosa_SKL-U AIO


Rev
-1

Date: **Wednesday, July 01, 2015** Sheet **69** of **105**

Blanking

www.teknisi-indonesia.com


<Variant Name>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title 070_(Reserved)		
Size A4	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015		Sheet 70 of 105

Blanking

www.teknisi-indonesia.com

<Variant Name>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title 071_(Reserved)		
Size A4	Document Number Rosa_SKL-U AIO	Rev -1
Date:	Wednesday, July 01, 2015	Sheet 71 of 105


Blanking

www.teknisi-indonesia.com

Blanking

www.teknisi-indonesia.com

<Variant Name>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title 073_(Reserved)		
Size A4	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015		Sheet 73 of 105

Blanking

www.teknisi-indonesia.com

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title **074_(Reserved)**

Size	Document Number
A	Rosa_SKL-U AIO


Rev
-1

Date:	Wednesday, July 01, 2015	Sheet	74	of	105
-------	--------------------------	-------	----	----	-----

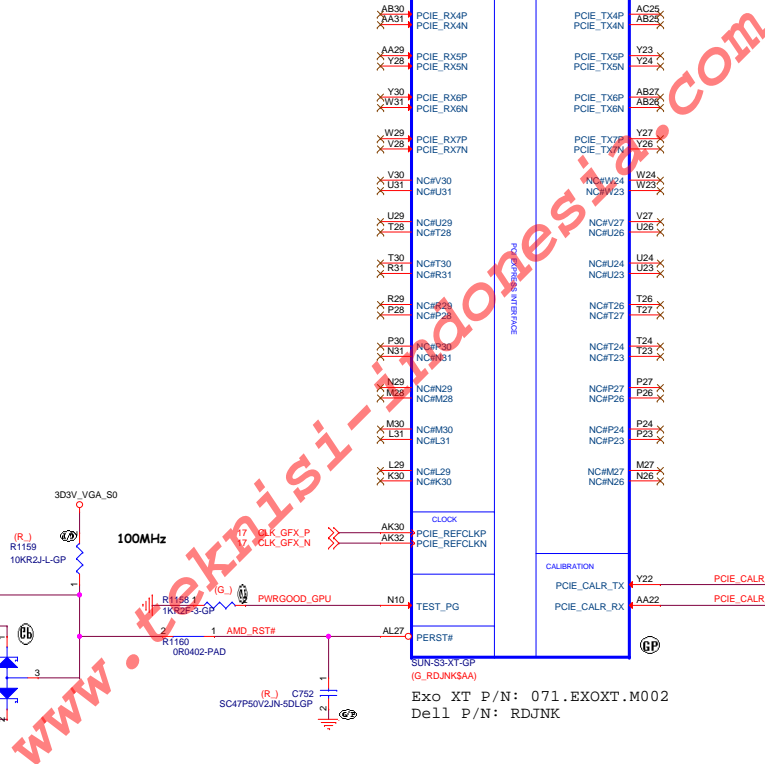
Blanking

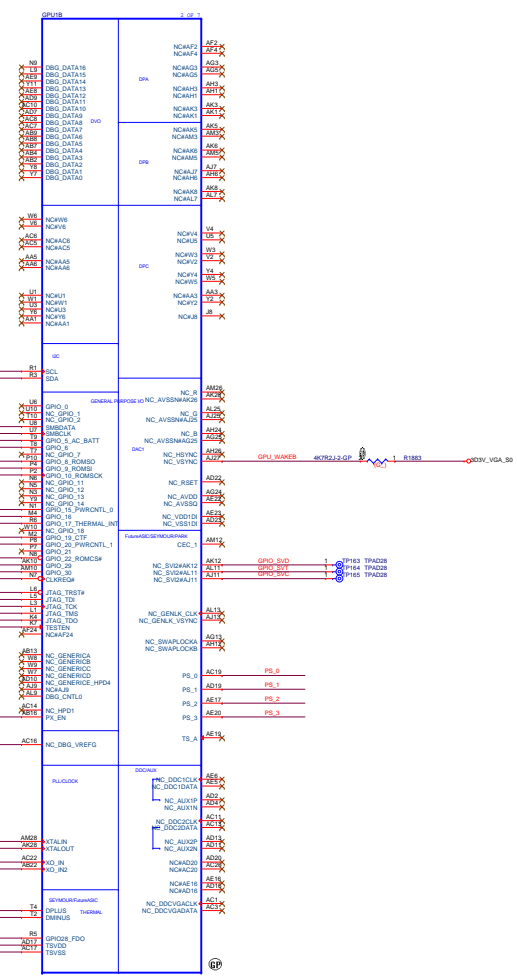
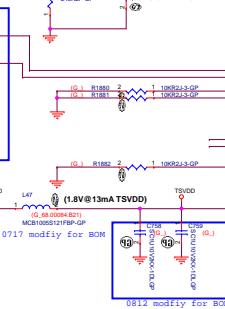
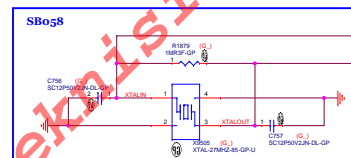
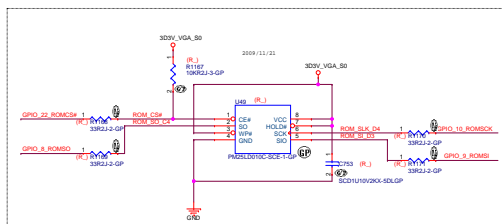
www.teknisi-indonesia.com

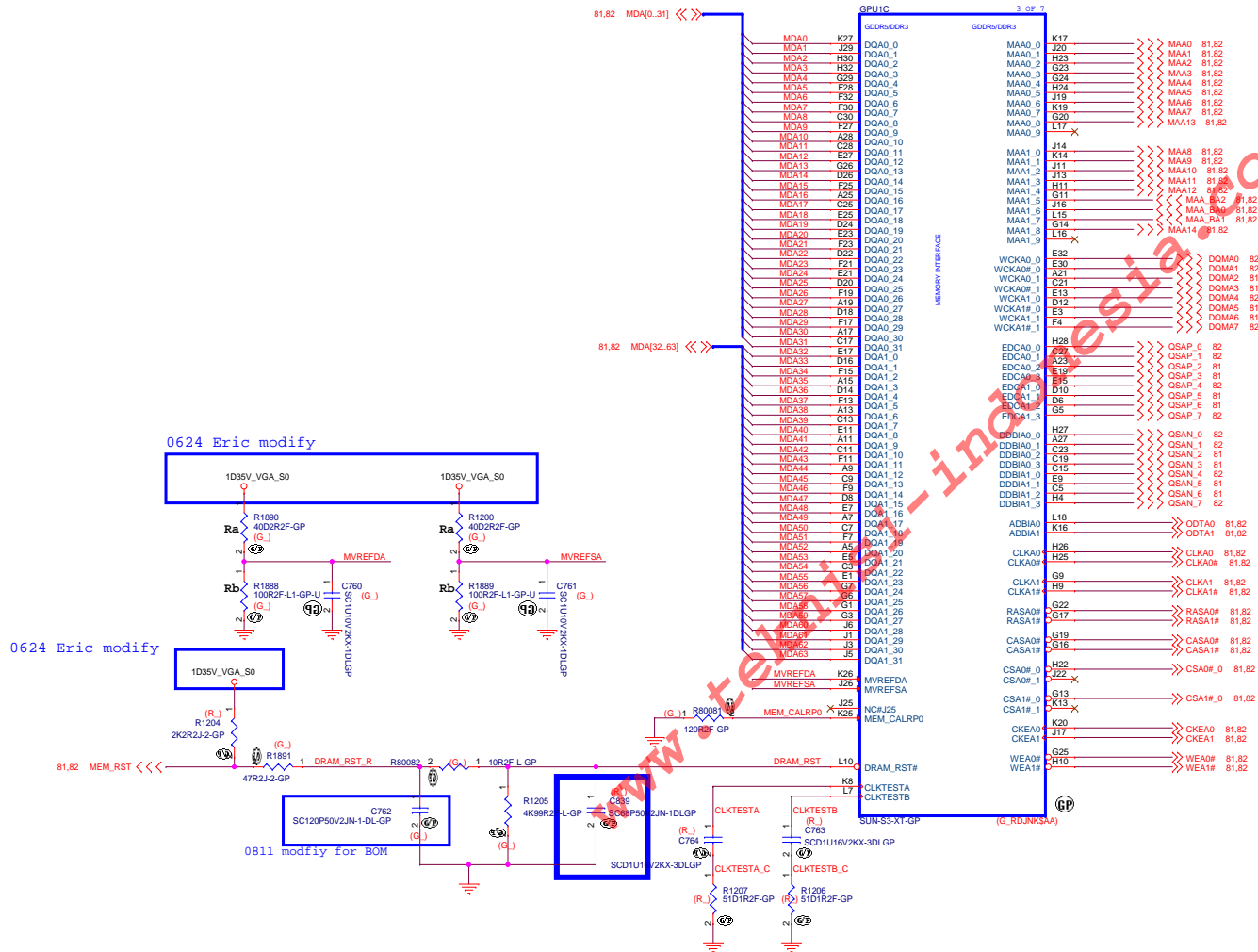
<Variant Name>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title 075_(Reserved)		
Size A4	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015		Sheet 75 of 105

24,76,79 PLTRST_SL_N >>————







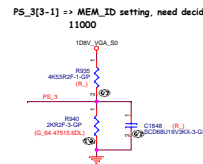
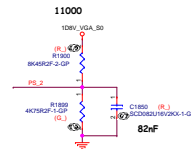
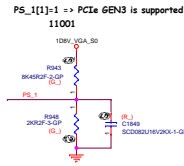
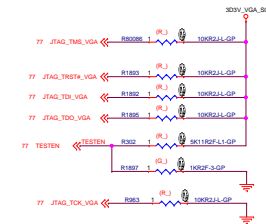


Table 3–22 Resistor Divider Lookup Table for Bits [3:1]

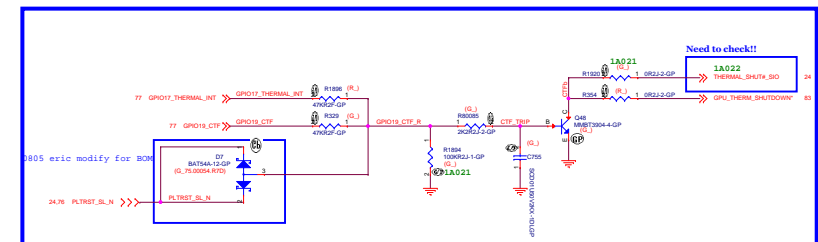
R _{pu} (Ω)	R _{pd} (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010

Signal	Normal mode	Debug mode	pilot r mode
TESTEN	"0" (PD)	"1" (PU)	"0" (PD)
JTAG_TEST#	"1" (PU)	"1" (PU)	NC
JTAG_TCK	"0" (PD)	"1" (PU)	NC
JTAG_TMS	"1" (PU)	"1" (PU)	NC



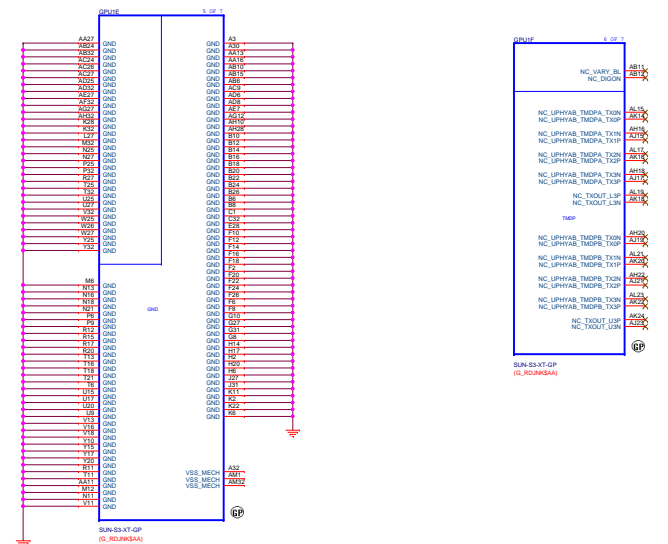
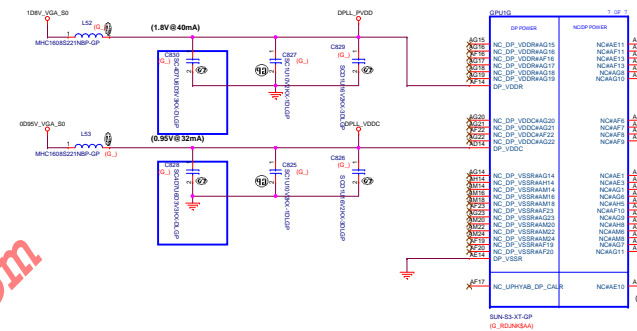
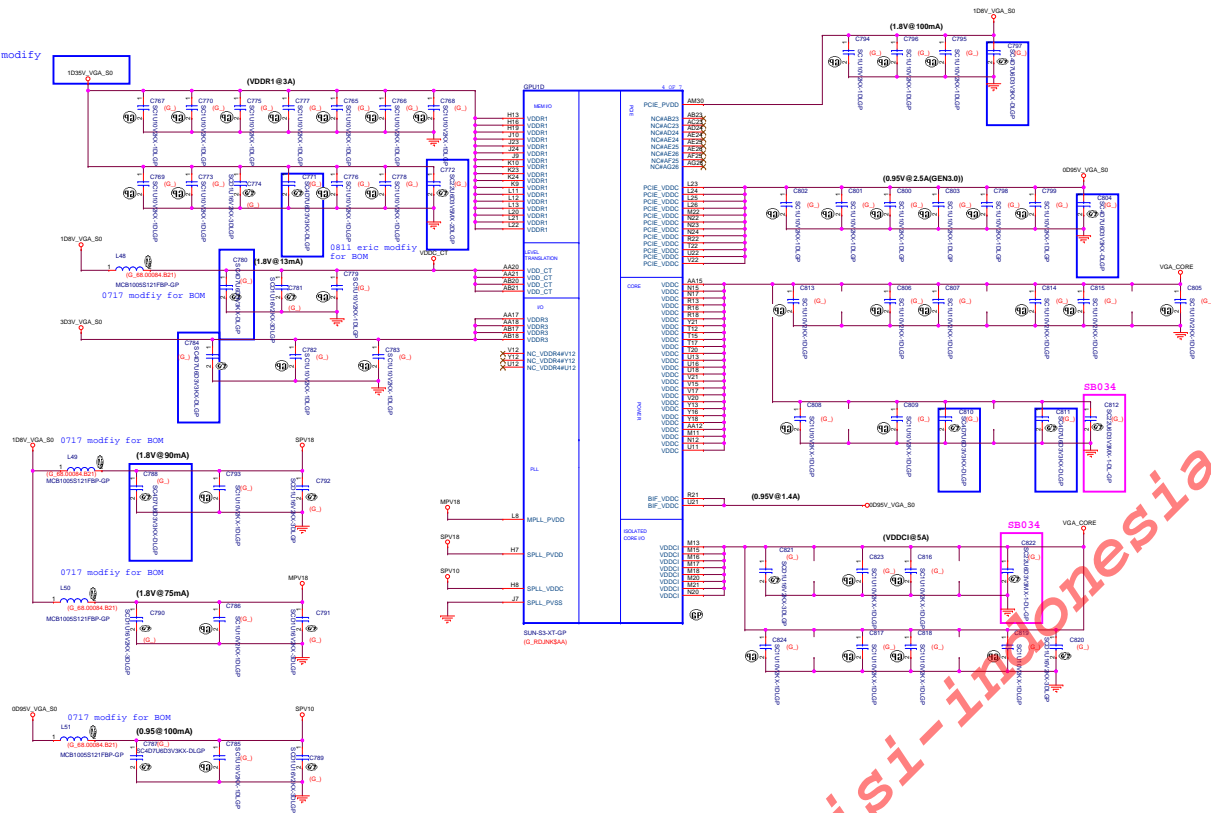
PS_2[4]	STRAP_BIF_VGA_DIS	VGA disable determines whether or not the card will be recognized as the system's VGA controller (through the SUBCLASS field in the PCI configuration space). 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_2[5] PS_0[4]	N/A	Reserved	N/A
		Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_ PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	Design dependent on the description

PS_3[11]	BOARD_CONFIG[0]	Board configuration related strapping, such as for memory, I/O, and design dependent, see the description.	Design dependent, see the description.
PS_3[12]	BOARD_CONFIG[1]		
PS_3[13]	BOARD_CONFIG[2]		
		Determines the maximum number of digital display audio endpoints that will be presented to the user. This should be set to the maximum number of digital display audio outputs that can be enabled simultaneously at the product, which is limited by the ASIC silicon itself, the number and type of connectors on the board (DP, HDMI), and the number of sinks for each I/O connector (the DP MST link policy of the video driver). Unused sinks should be disabled. This pin must be encoded as an active low signal as follows to ensure zero enables all endpoints.	
PS_3[14]	AUD_PORT_CONN_PINSTRAP[1]		
	AUD_PORT_CONN_PINSTRAP[2]		
PS_3[15]		<p>11 = No usable endpoints.</p> <p>110 = One usable endpoint.</p> <p>101 = Two usable endpoints.</p> <p>100 = Three usable endpoints.</p> <p>011 = Four usable endpoints.</p> <p>010 = Five usable endpoints.</p> <p>001 = Six usable endpoints.</p> <p>000 = All endpoints are usable.</p>	Design dependent, see the description.



THERMAL PROTECTION

0624 Eric modify



For cost effective designs,

VDDCI and VDDC can share one common regulator

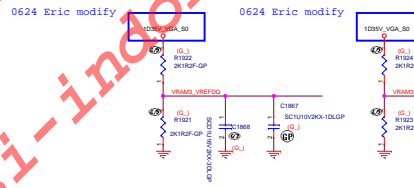
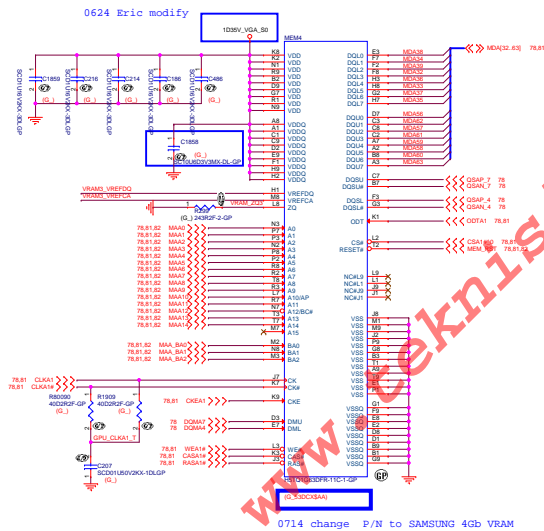
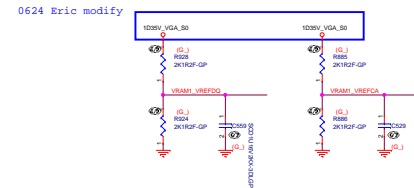
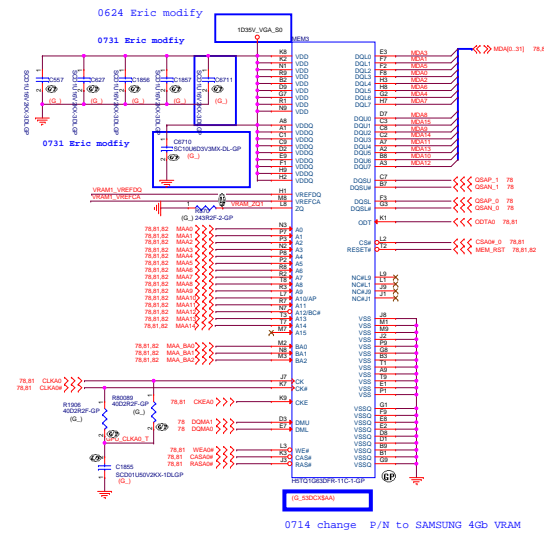
supplying the total TDC of both rails

VDDC and VDDCI vias should be separate underneath the ASIC and only joined on the unified power plane

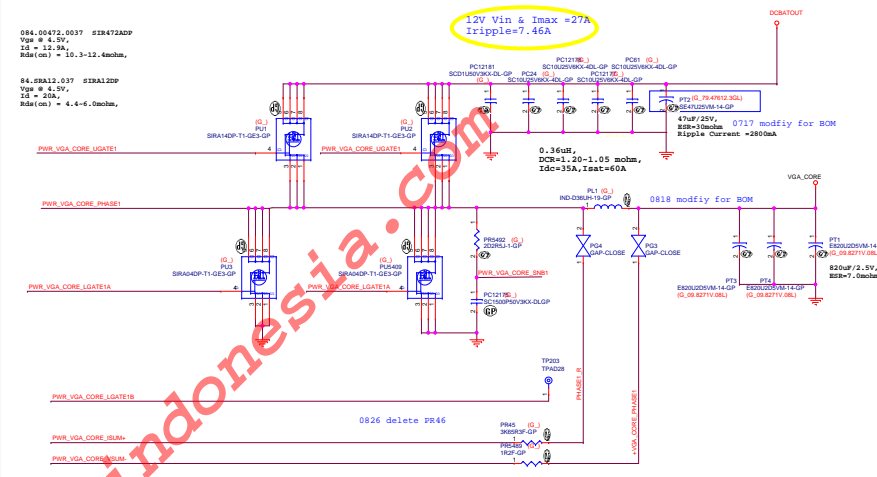
For designs that target maximal performance,


a dedicated regulator for VDDCI with two selectable output levels is required.

VDDCI FB is available on Topaz.



256M*16 VRAM
 53DCX5AA - SAMSUNG K4W4G1646E-BC1A
 PP8TP5AA - Micron MT41J256M16HA-093G:E
 W5PXV5AA - Hynix H5TC4G63CFR-N0C

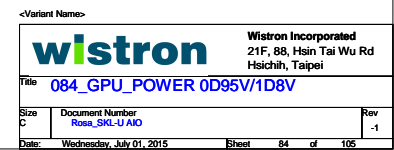


 <div> <p>Wistron Incorporated</p> <p>21F, 88, Hsin Tai Wu Rd</p> <p>Hsichih, Taipei</p> </div>	
<p>File: 083_GPU_POWER CORE</p>	
Size	Document Number
D	Rosa_SKL_AIO
<p>Wistron SKL_AIO</p>	

RT8068 for 0D95_VGA

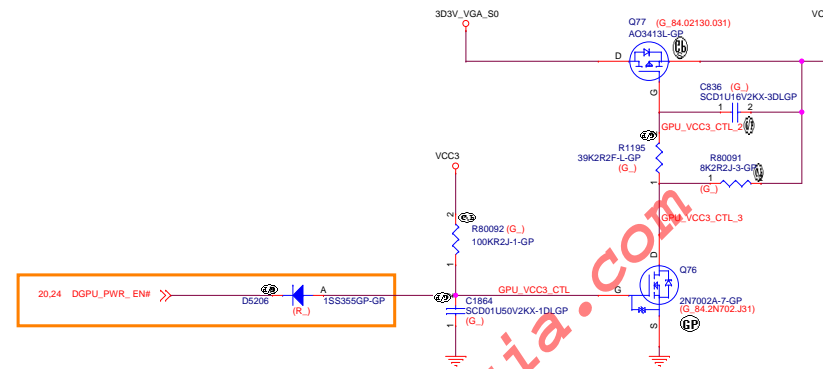


RT6220 for 1D8V_S0

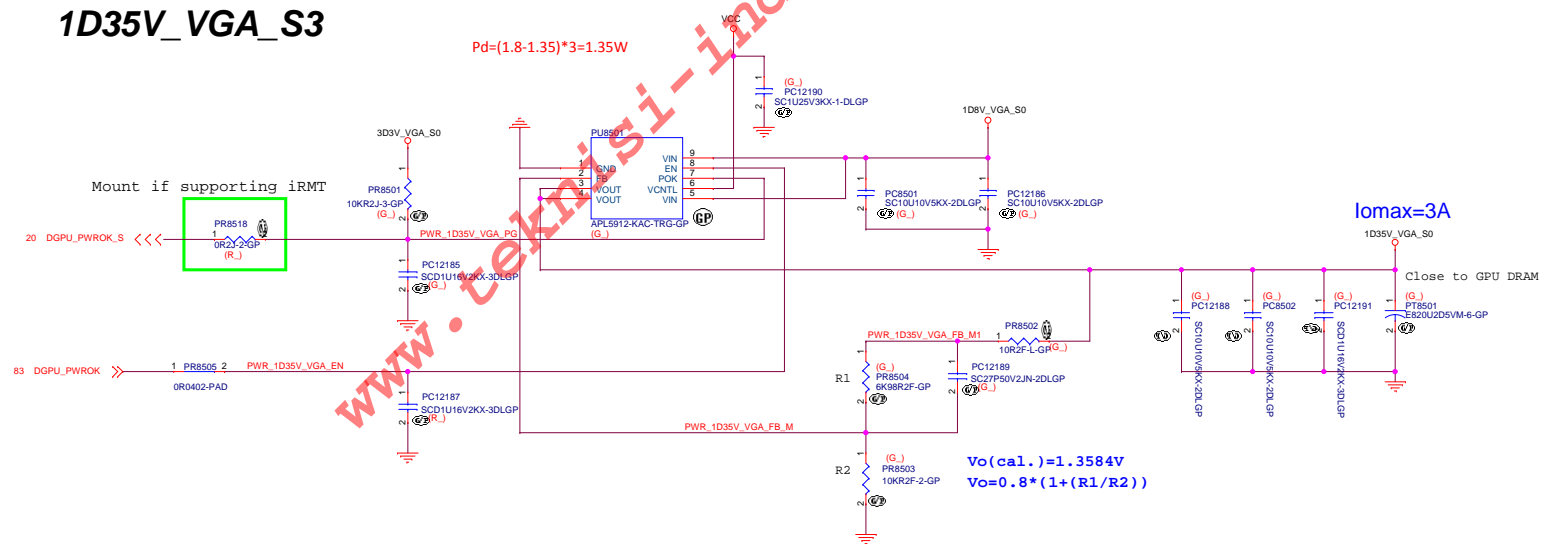


0528 Eric modify from victoria

3D3V_S0 to 3D3V_DELAY Transfer



1D35V_VGA_S3




<Variant Name>

Blanking

www.teknisi-indonesia.com

Blanking

www.teknisi-indonesia.com

<Variant Name>			
		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title 087_(Reserved)			
Size B	Document Number Rosa_SKL-U AIO		Rev -1
Date:	Wednesday, July 01, 2015	Sheet 87 of 105	

Blanking

www.teknisi-indonesia.com

<Variant Name>



Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title **088_(Reserved)**

Size **B** Document Number **Rosa_SKL-U AIO**


Rev **-1**

Date: Wednesday, July 01, 2015 Sheet 88 of 105

Blanking

www.teknisi-indonesia.com

<Variant Name>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title 089_(Reserved)		
Size A4	Document Number Rosa_SKL-U AIO	Rev -1
Date:	Wednesday, July 01, 2015	Sheet 89 of 105

Blanking

www.teknisi-indonesia.com

<Variant Name>



Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title **090_(Reserved)**

Size A4	Document Number Rosa_SKL-U AIO	Rev -1
------------	--	-----------

Date: Wednesday, July 01, 2015 Sheet 90 of 105

Blanking

www.teknisi-indonesia.com

<Variant Name>



Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title 091_(Reserved)

Size Custom	Document Number Rosa_SKL-U AIO	Rev -1
-------------	--------------------------------	--------

Date: Wednesday, July 01, 2015	Sheet 91 of 105
--------------------------------	-----------------


Blanking

www.teknisi-indonesia.com

Blanking

www.teknisi-indonesia.com


<Variant Name>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title 093_(Reserved)		
Size A4	Document Number Rosa_SKL-U AIO	Rev -1
Date:	Wednesday, July 01, 2015	Sheet 93 of 105

Blanking

www.teknisi-indonesia.com


<Variant Name>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title 094_(Reserved)		
Size A4	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015		Sheet 94 of 105

Blanking

www.teknisi-indonesia.com


<Variant Name>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title 095_(Reserved)		
Size A4	Document Number Rosa_SKL-U AIO	Rev -1
Date:	Wednesday, July 01, 2015	Sheet 95 of 105

Blanking

www.teknisi-indonesia.com

<Variant Name>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title 096_(Reserved)			
Size A4	Document Number Rosa_SKL-U AIO		Rev -1
Date:	Wednesday, July 01, 2015	Sheet 96 of 105	

Blanking

www.teknisi-indonesia.com

<Variant Name>



Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title **097_(Reserved)**


Size A4	Document Number Rosa_SKL-U AIO	Rev -1
------------	--	-----------

Date: Wednesday, July 01, 2015 Sheet 97 of 105

Blanking

www.teknisi-indonesia.com

<Variant Name>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title 098_(Reserved)		
Size A4	Document Number Rosa_SKL-U AIO	Rev -1
Date: Wednesday, July 01, 2015		Sheet 98 of 105

Layout Note:

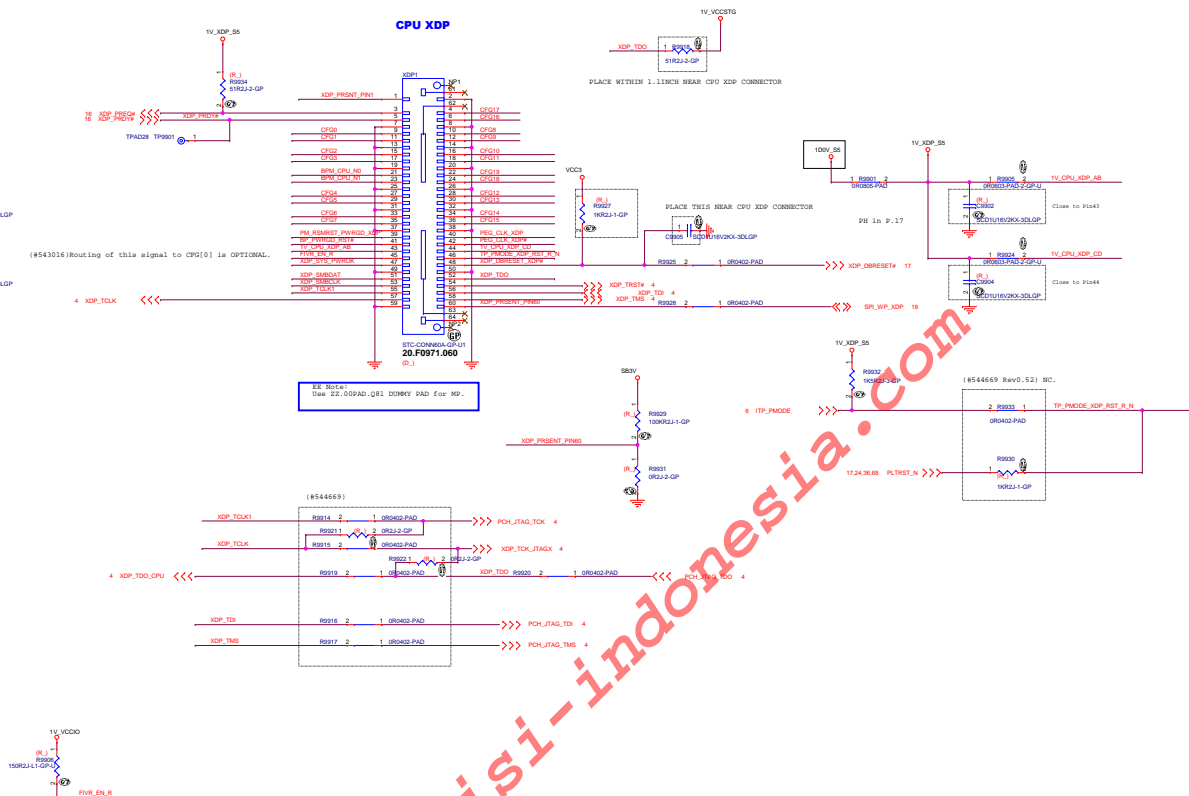
Layout Note:



12,13,18,55,67,77	SMB_DATA_MAIN	R0911	2	1	GRD402-PAD	XDP_SMBDAT
12,13,18,46,67,77	SMB_CLK_MAIN	R0912	2	1	GRD402-PAD	XDP_SMBCLK

17 PEG_CLK_CPU R9213 2 1 GRM02-PAD PEG_CLK_XDP
18 PEG_CLK_CPU R9223 2 1 GRM02-PAD PEG_CLK_XDP#

6 CFG[19:0] <<> CFG[19:0]
4 BPM_CPU_N[1:0] <<> BPM_CPU_N[1:0]



Blanking

www.teknisi-indonesia.com

<Variant Name>



Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title **100_(Reserved)**

Size A4	Document Number Rosa_SKL-U AIO	Rev -1
------------	--	-----------

Date: Wednesday, July 01, 2015 Sheet 100 of 105

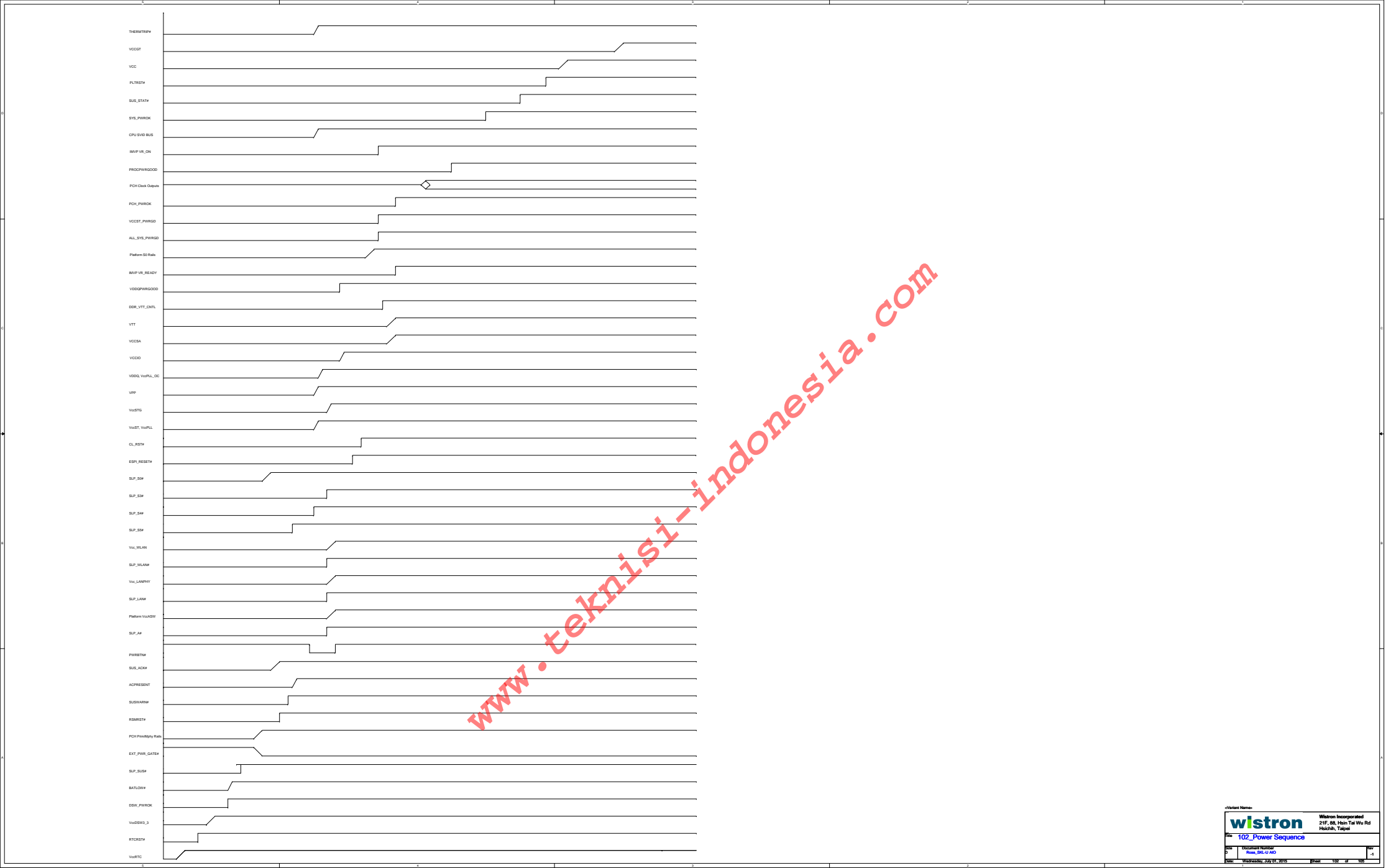
6-1.2-7c(2.40) stack up and impedance

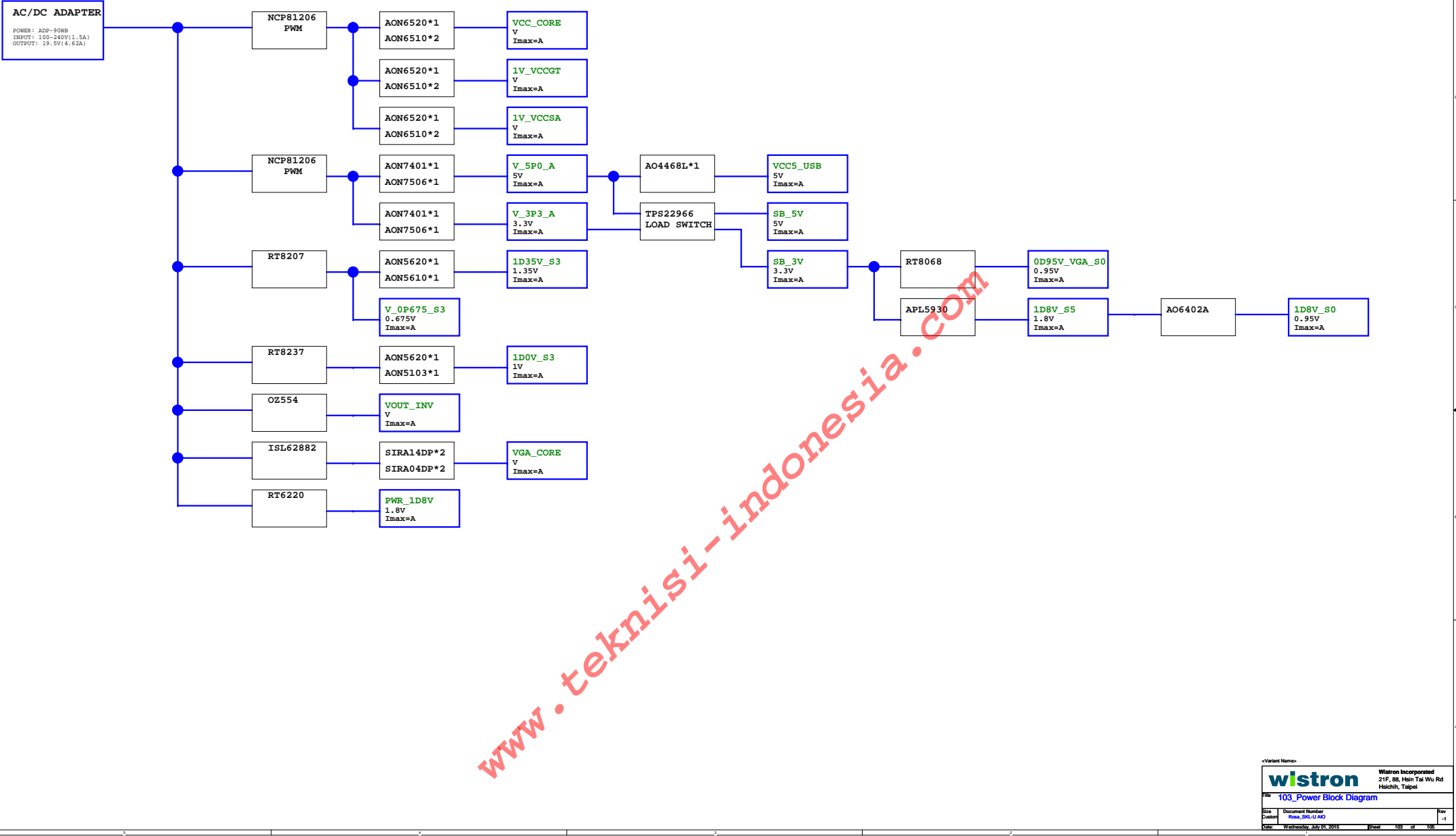
叠层編號	6-1.2-7c	注意事項	1. Impedance Control tolerance $\pm 10\%$
完成板厚 (mm)	1.2 \pm 0.12		2. Coupon 製作方式及 Impedance report 請依照 Wistron 規範製作

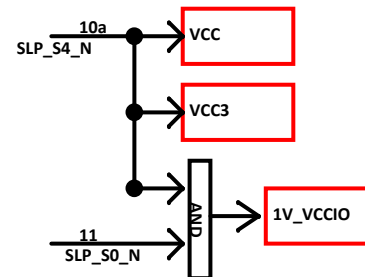
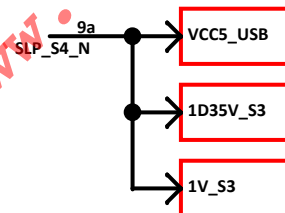
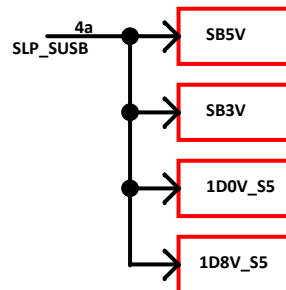
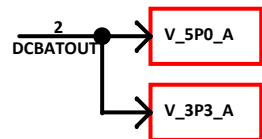
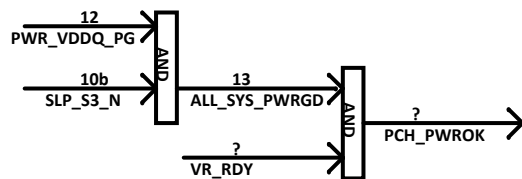
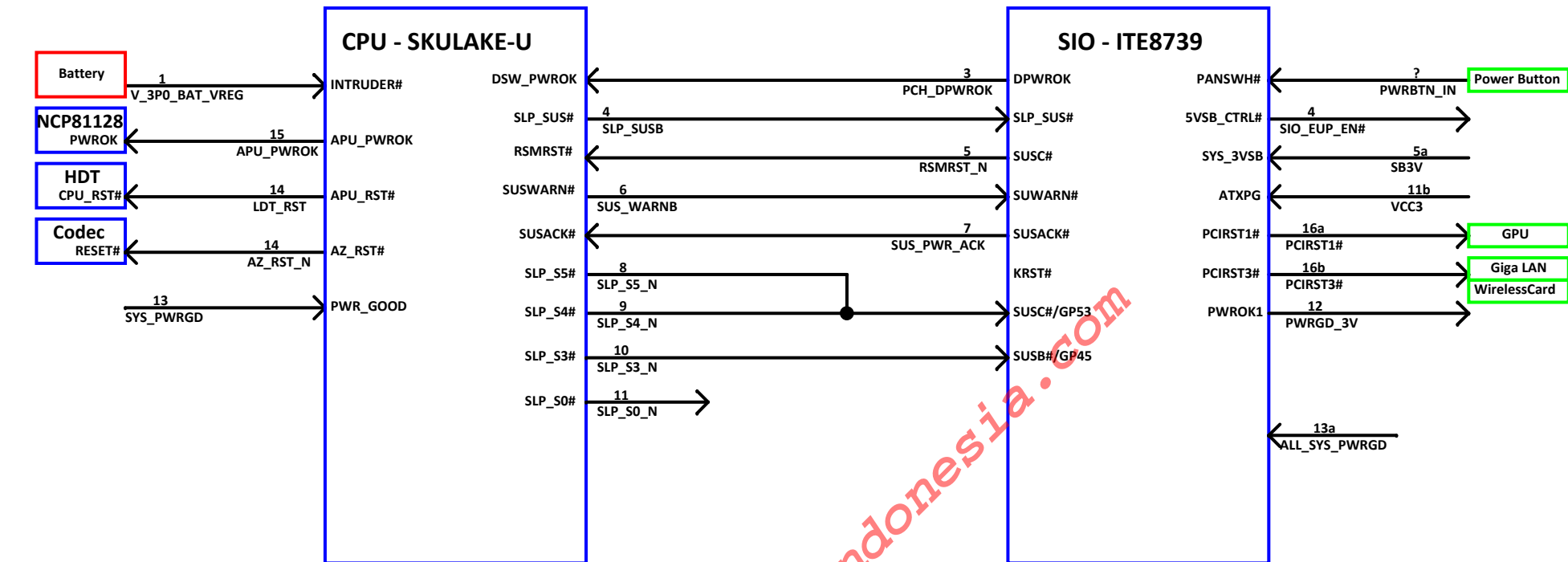
Stack up			Impedance Request List				
Layer	Spec	Thickness (mil)	Single Ended Type (Trace width : mil)				
			L1 (Ref. Plane) ^{※ 1}	L3 (Ref. Plane)	L4 (Ref. Plane)	L6 (Ref. Plane)	
L1	TOP	PP	27.4 Ω	12.0 (L2)	16.0 (L2/L5)	12.0 (L5)	
L2	G/P ^{※ 3}	Core	33 Ω	9.0 (L2)	12.0 (L2/L5)	9.0 (L5)	
L3	Signal	PP	34 Ω	8.5 (L2)	11.5 (L2/L5)	8.5 (L5)	
L4	Signal	Core	35 Ω	8.0 (L2)	10.5 (L2/L5)	8.0 (L5)	
L5	G/P	PP	37.5 Ω	7.0 (L2)	9.5 (L2/L5)	7.0 (L5)	
L6	Bottom	PP	39 Ω	6.5 (L2) ^{※ 4}	9.0 (L2/L5)	6.5 (L5) ^{※ 4}	
			40 Ω	6.5 (L2) ^{※ 4}	8.5 (L2/L5)	6.5 (L5) ^{※ 4}	
			42 Ω	5.5 (L2)	7.5 (L2/L5)	5.5 (L5)	
			45 Ω	5.0 (L2)	6.5 (L2/L5)	5.0 (L5)	
			48 Ω	4.5 (L2)	5.5 (L2/L5)	4.5 (L5)	
			50 Ω	4.0 (L2)	5.0 (L2/L5)	4.0 (L5)	
			52 Ω	3.5 (L2) ^{※ 2}	4.5 (L2/L5)	3.5 (L5) ^{※ 2}	
			55 Ω	NA	4.0 (L2/L5)	NA	
Differential Type (Trace width/Space width/Trace width: mil)							
110 Ω	NA	3.5/13/3.5 (L2/L5)	3.5/13/3.5 (L2/L5)	NA			
100 Ω	3.5/10/3.5 (L2)	4/9/4 (L2/L5)	4/9/4 (L2/L5)	3.5/10/3.5 (L5)			
95 Ω	3.5/6/3.5 (L2); 4/10/4 (L2)	4/6/4 (L2/L5)	4/6/4 (L2/L5)	3.5/6/3.5 (L5); 4/10/4 (L5)			
93 Ω	3.5/5/3.5 (L2); 4/8/4 (L2)	4/5/4 (L2/L5); 5/9/5 (L2/L5)	4/5/4 (L2/L5); 5/9/5 (L2/L5)	3.5/5/3.5 (L5); 4/8/4 (L5)			
90 Ω	4/6/4 (L2)	4/5/4 (L2/L5); 5/8/5 (L2/L5)	4/5/4 (L2/L5); 5/8/5 (L2/L5)	4/6/4 (L5)			
85 Ω	4/4.5/4 (L2); 5/8/5 (L2)	5/5/5 (L2/L5); 5/5/5 (L2/L5)	5/5/5 (L2/L5); 5/5/5 (L2/L5)	4/4.5/4 (L5); 5/8/5 (L5)			
80 Ω	5/5/5 (L2)	6/6/6 (L2/L5)	6/6/6 (L2/L5)	5/5/5 (L5)			
75 Ω	6/6/6 (L2)	7/6/7 (L2/L5)	7/6/7 (L2/L5)	6/6/6 (L5)			
72 Ω	7/6/7 (L2)	7/5/7 (L2/L5)	7/5/7 (L2/L5)	7/6/7 (L5)			
70 Ω	7/6/7 (L2)	8/6/8 (L2/L5)	8/6/8 (L2/L5)	7/6/7 (L5)			
68 Ω	6.5/4/6.5 (L2)	7.5/4/7.5 (L2/L5)	7.5/4/7.5 (L2/L5)	6.5/4/6.5 (L5)			
65 Ω	8/6/8 (L2)	9/5/9 (L2/L5)	9/5/9 (L2/L5)	8/6/8 (L5)			
Remark:							
※ 1: "Ref. Plane" means the reference plane of the traces.							
※ 2: Trace space should be wider than 4.0mil (Wistron internal only).							
※ 3: G is GND, P is PWR							
※ 4: Only choose one signal trace width on layer L1&L6							
Total	45.6						

<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title		101_PCB STACKUP	
Size	Document Number	Rev	
B	Rosa_SKL-U A10	-1	
Date:	Wednesday, July 01, 2015	Sheet	101 of 105







0

C

B

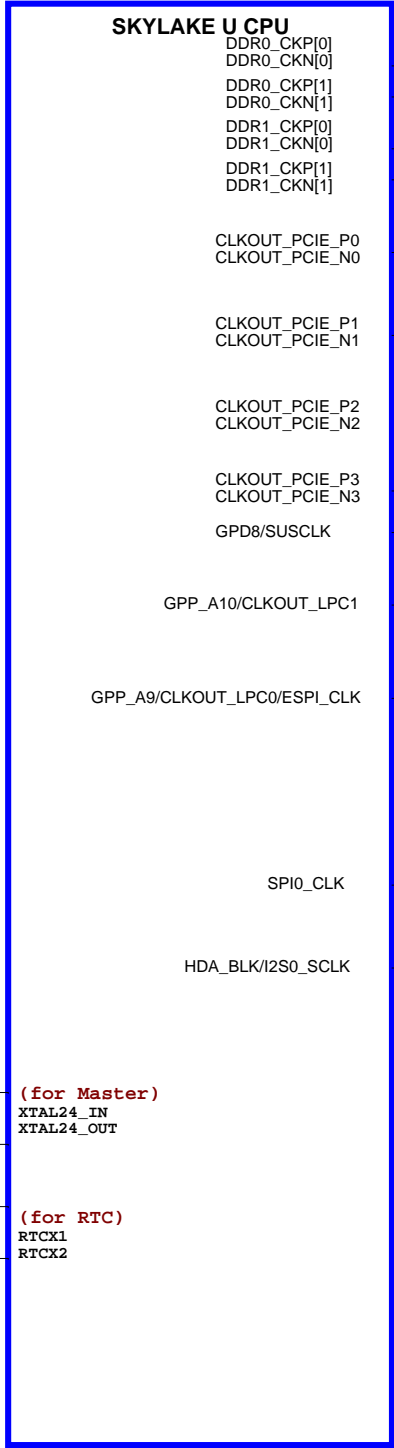
A

0

C

B

A



M_A_CLK0/M_A_CLK#0

M_A_CLK1/M_A_CLK#1

M_B_CLK0/M_B_CLK#0

M_B_CLK1/M_B_CLK#1

CLK_GFX_P/CLK_GFX_N
100MHz

CLK_GLAN_P/CLK_GLAN_N
100MHz

CLK_WLAN_P/CLK_WLAN_N
100MHz

CLK_CR_P/CLK_CR_N
100MHz
SUS_CLK

LPC_CLK1
33MHz

LPC_CLK0
33MHz

SPI_CLK
24MHz/48MHz/100MHz

AUD_LINK_BCLK

DIMM1

DIMM2

GPU(AMD EXO)

LAN RTL8111H

NGFF A-key WLAN+BT

CARD READER
RTS5227S

SIO IT8739

EC NPCE948LA0DX

LPC DEBUG PORT

SPI ROM

AUDIO ALC3661

SCALAR
RTD2586HD

X9505
27MHz

X4
25MHz

OSC2
48MHz

X9502
14.31818MHz

X9503
24MHz
(for Master)
XTAL24_IN
XTAL24_OUT

X9504
32.768KHz
(for RTC)
RTCX1
RTCX2

www.teknisi-indonesia.com